Very Fast Transient Voltage Regulators Based on Load Correction

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Abstract — The requirement of output current of very high slew rate has presented great challenge to the design of voltage regulator modules that deliver power to computer CPUs such as the Pentium Pro. Methods for enhancing transient speed have been evolved around the reduction of effective inductance of the switching regulator through interleaving and paralleling converters. This paper introduces the concept of “phantom load” for achieving very fast and tight output voltage regulation for any switching converter. Essentially a special load corrector circuit is attached to the output of the switching regulator. This load corrector combines with the actual load (e.g., CPU chip) to form a slowly varying composite load or “phantom load” which permits the switching regulator to maintain a well regulated output voltage even when the actual load is changing very rapidly. This paper discusses the conceptual construction of the load corrector and its practical implementations. Experimental tests (based on available IC and discrete components) for a 20A step load showing an output voltage fluctuation of less than ±30mV are presented.

I. INTRODUCTION

The performance of typical switching converters in respect of transient response is deemed not satisfactory in applications where high slew rates of output current are demanded. Although it is theoretically possible to achieve very fast transient response by operating the switching converter at a very high frequency (hence very small inductance), practical switching devices impose a limit to the operating frequency [1]. Consequently, switching converters employing feedback control for output regulation or programming can only cope with relatively slowly changing load current. In the case of output voltage regulation, when the need arises for very fast transient response, a post-regulator is used which is invariably a linear regulator. Linear regulators, though having very fast transient response, continuously dissipate power, resulting in significant reduction of the overall power supply efficiency.

Low-voltage power supplies for integrated circuits, which encompass a wide range of applications including computer CPUs and communication equipment, require an extremely high slew rate of output current and yet a very well regulated voltage.

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II. THE PROBLEM AND OBJECTIVE OF THE PAPER

Before we attempt to develop design methods to meet the voltage supply requirement of computer CPUs, we review the basic problems associated with the design of voltage regulators for such applications.

Problem 1 Since the actual apparatus (e.g., CPU chip) is located at a distance from the voltage regulator, the very high load current slew rate (if it is met) will induce significant voltage spike due to the parasitic inductance connecting the voltage regulator output and the apparatus. A possible fix is to place large decoupling capacitance in the close proximity of the apparatus [2, 3], as shown in Figure 1. Of course, a voltage spike will still be present due to resonance between the decoupling capacitance and the package impedance, but this spike (called “first spike” in [2, 3]) can be controlled by the size of the decoupling capacitance.

Problem 2 The voltage regulator module (VRM) cannot respond fast enough to meet the voltage regulation and loading requirement. It has been shown [2], for the case of a Pentium Pro mother board, that the VRM needs to maintain a voltage fluctuation of less than ±2% in order to meet the ±5% requirement for the CPU in the event of a fast (4A/ns) load current.

Our attention is focused on Problem 2. Since the transient response of a switching converter is limited by the operating frequency and ultimately by the size of the converter inductance, there is a practical performance limit to which any feedback control scheme, however sophisticated, can ultimately achieve. Recently, methods for enhancing transient speed of voltage regulators have been proposed by reducing the effective inductance of the switching regulator through interleaving and paralleling converters [2, 4, 5]. Such methods are effective, but expensive.

This paper discusses an effective low-cost design of voltage regulators that can provide very fast transient response meeting the requirements of future microprocessors, without degradation of the overall efficiency of the power supply. The theory of the method was described in Tse-Poon [6], and active element realization was pursued on the basis of RC-nullor circuits. This paper presents the subject from a practical perspective.
III. LOAD CORRECTOR AND THE "PHANTOM LOAD" CONCEPT

We begin by introducing a new element called load corrector (LdCr) which is a circuit that attaches to the output terminals of a switching regulator. Together the LdCr and the load form a composite or "phantom" load for the switching converter. The LdCr is capable of responding to any fast changing load by supplying the necessary amount of transient current at an arbitrarily high speed. The "phantom" load, which is the effective load observed by the switching converter, is made to change sufficiently slowly such that the switching converter is able to provide a well regulated output voltage. The approach is unconventional in the sense that no feedback scheme is employed to modulate the duty cycle of the switching converter.

Figure 2: Conceptual construction of the load corrector circuit

The LdCr can be conceptually constructed based on either voltage sensing or current sensing, as shown in Figure 2.

Case 1: Voltage Sensing — In the case of voltage sensing, the output voltage of the load is sensed, and any minute difference between the sensed voltage and the nominal value will trigger a bi-directional controlled current source to inject the right amount of current to the load.

Alternatively, the rate of fluctuation of the output voltage is sensed. In the event of fast changing load, the bi-directional controlled current source is triggered to inject the right amount of current to the load, the purpose being to limit the rate of fluctuation of the output voltage. The fast triggering is made possible by virtue of active devices in the absence of reactive elements. The output voltage will then be brought immediately back to the nominal value.

Case 2: Current Sensing — In the case of current sensing, the current supplying the "phantom" load is sensed, and its rate of change is limited or controlled by the action of the LdCr such that the switching regulator is capable of providing well regulated output voltage. Thus, the LdCr serves to limit or control the rate of change of current demanded by the phantom load as well as to supply current to the load at an arbitrarily fast rate.

In summary, the following features distinguish the proposed method from other kinds of compensation techniques:

1. The LdCr integrates with the load to produce a corrected load for the switching converter. The switching converter deals no longer with fast changing load, and hence can readily manifest itself as a "stiff" voltage source, maintaining a well regulated output voltage as required by the application concerned.

2. Unlike a linear regulator which continuously dissipates power, the LdCr consumes a very small amount of power. The LdCr is designed to supply zero current in the steady state when the load is constant. In the extreme event of an abrupt jump in load current demand, the LdCr supplies a current pulse momentarily to the load. The switching converter eventually supplies all of the load current, and the duration of time in which the LdCr supplies current is vanishingly small. Hence, with almost zero conduction time, the LdCr consumes very little power. Figure 3 shows the essential current waveforms.

3. The LdCr is independent of the switching converter, and hence can be designed and manufactured separately as a "plug-on" circuit.

IV. PRACTICAL FORMS OF LOAD CORRECTOR CIRCUITS

In this section we describe some practical forms of implementing the LdCr based on voltage and current sensing, as conceptually outlined above.

A. Based on Sensing $V_{out}$

The sensor continuously observes the output voltage, compares it with a reference voltage, and sends a driving signal to the bi-directional controlled current source which supplies current to the load according to the sign and magnitude of the difference between the sensed voltage and the reference. The bi-directional controlled current source ceases to supply current when the magnitude of the output voltage equals the reference level. Figure 4 (a) shows a simplified schematic of the voltage-sense LdCr.
Figure 3: Essential current waveforms. Left: actual load current; Middle: current supplied by LdCr; Right: current supplied by voltage regulator

![Waveforms](image)

Figure 4: Load corrector based on (a) voltage-sense; (b) voltage-rate-sense

![Corrector Diagrams](image)

Figure 5: Load corrector based on current-rate-sense

![Corrector Diagrams](image)

B. Based on Sensing \( \frac{dV_{out}}{dt} \)

Instead of sensing the output voltage, the sensor may sense the rate of change of the output voltage (effectively a high-pass filter). The object is to "clamp" this rate of change to almost zero by injecting or sinking current at arbitrarily fast rate to the load during transient. A simplified schematic is shown in Figure 4 (b). In this form of LdCr, a special requirement must be incorporated with care, which addresses the possible "race situation" that exists between the LdCr and the voltage regulator module. Essentially the LdCr should not permanently supply current to the load after a transient, but should allow the voltage regulator to take care of all load current at a rate that can be handled by the voltage regulator.

C. Based on Sensing \( \frac{dI_{out}}{dt} \)

The sensor senses the rate of change of the current that is being supplied by the switching converter. In the event of a very abrupt load change, the LdCr circuit limits the rate of change of the output current of the switching regulator by commanding the bi-directional controlled current source to inject the necessary amount of current to the load. The circuit thus typically comprises a high-pass filter circuit, a simplified schematic of which is shown in Figure 5. In this case, no voltage reference is needed.

Remarks — All three forms of LdCr can be implemented using active devices. The sensor part may employ op-amps and passive devices, and the bi-directional current source may employ MOSFETs connected in a typical push-pull configuration. Also, in practice, a narrow tolerance band may be required in the comparator in order to prevent continuous latching due to the finite output voltage (or current) ripple. It is worth noting that LdCr's based on sensing \( \frac{dv}{dt} \) and \( \frac{di}{dt} \) represent more practical forms of implementation, because they can be constructed fully independently without the need for a voltage reference or the need for adjusting a reference.

V. ANALYSIS OF OUTPUT VOLTAGE TRANSIENT

In this section we present a simple analysis of the output voltage transient when the output current is rapidly rising. Our main purpose here is to compare the two cases with and without the use of LdCr. We will focus on the mechanism whereby output voltage fluctuation is kept within the specified limit. We begin with the following assumptions:

![Schematic](image)
Figure 7: MathCad simulated output voltage across output decoupling capacitor which is composed of $N$ capacitors in parallel, each with $C = 260 \mu \text{F}$, $R_{\text{ser}} = 0.3 \text{m}\Omega$ and $L_{\text{ser}} = 0.01 \text{nH}$. The output current is stepping from 0 to 50A, slewing at 150A/µs.

(a) $N = 1$; (b) $N = 50$.

1. The output capacitor connected to the output of the voltage regulator is composed of the intended capacitance $C$, plus parasitic resistance $R_{\text{ser}}$ and lead inductance $L_{\text{ser}}$, as shown in Figure 6.

2. The immediate output current is given by the following piecewise linear function:

$$i_{\text{out}}(t) = \begin{cases} \frac{I_o t}{t_c} & \text{for } 0 < t < t_c \\ \frac{I_o}{t_c} & \text{for } t \geq t_c \end{cases}$$

(1)

where $I_o$ is the current step and $t_c$ defines the slewing period which is much shorter than the normal transient time of the voltage regulator.

3. If a LdCr is attached to the output (terminals AB in Figure 6), the output voltage will be clamped after $t_s$ sec depending on the delay of the LdCr. Effectively we are saying that once the LdCr starts to respond, the output voltage is clamped.

The immediate output current $i_{\text{out}}$ is pumped into the output capacitor very rapidly as given by (1). In the absence of any LdCr and before the “slow” voltage regulator can respond, the output voltage $v_c(t)$ is given by

$$v_c(t) = \int_0^t \frac{i_{\text{ser}}(t)}{C} \, dt + L_{\text{ser}} \frac{di_{\text{ser}}(t)}{dt} + R_{\text{ser}} i_{\text{out}}(t)$$

$$= \begin{cases} \frac{I_o t^2}{2 t_c} + \frac{L_{\text{ser}} I_o}{t_c} + \frac{R_{\text{ser}} I_o}{t_c} & \text{for } 0 < t < t_c \\ \frac{I_o t^2}{2 C} + \frac{L_{\text{ser}} (t - t_c)}{C} + \frac{R_{\text{ser}} I_o}{t_c} & \text{for } t \geq t_c \end{cases}$$

(2)

Suppose the output current is defined by (1) with the following parameters:

$I_o = 50 \text{A}$, $\frac{di_{\text{out}}}{dt} = 150 \text{A/µs}$ (i.e., $t_c = 333.33 \text{ns}$)

Further suppose the output capacitor is composed of $N$ capacitors in parallel, each having the following parameters:

$$C = 260 \mu \text{F}, \quad R_{\text{ser}} = 0.2 \text{m}\Omega, \quad L_{\text{ser}} = 0.01 \text{nH}.$$
earlier, the demand on the size of decoupling capacitor at the VRM end is significantly reduced. However, we should stress that the decoupling capacitance on the load end (microprocessor or CPU) is still mandatory as explained previously in Section II.

VI. EXPERIMENTAL SETUP AND RESULTS

We will exemplify in this section the form of LdCr corresponding to $dv/dt$ sensing. In our experiment the LdCr is inserted at the output of the voltage regulator, as shown in Figure 8. The output capacitor of the voltage regulator is an OSCON electrolytic-type capacitor which has $C = 4000\mu\text{F}$, $R_{\text{er}} = 0.3\Omega$ and $L_{\text{er}} = 0.01\text{nH}$. The load is switched from 1A to full load at 21A. The voltage regulator output is 5V. The circuit schematic is shown in Figure 9 (a).

Figures 10 (a) and (b) show the output voltage during transient, corresponding respectively to the cases without and with the $dv/dt$ sense LdCr. As shown, the output voltage fluctuation is significantly reduced to $\pm 30\text{mV}$ when the LdCr is turned on. This fluctuation is independent of the output voltage level, and in this case corresponds to 0.6% of the 5V output, or 1% of a 3V output. Furthermore, Figure 10 (c) is a blow-up of the output voltage, showing the delay time of the LdCr which is about 424ns. From $t_1$ to $t_2$, the waveform is essentially governed by equation (2), and starting $t_2$ the voltage is clamped by the LdCr.

The op-amps used for the present experiment are AD817 which has $f_T = 50\text{MHz}$ and slew rate $350\text{V}/\mu\text{s}$ according to manufacturer's data. It is worth noting that the above-reported delay time can be further shortened if faster devices are used, and hence yet smaller decoupling capacitance at the regulator end can be used.

Finally, one may also construct another form of LdCr based on $di/dt$ sensing. A schematic is shown in Figure 9 (b). Some experimental results can be found in [6].

<table>
<thead>
<tr>
<th>Max. output volt. fluctuation</th>
<th>$\pm 30\text{mV}$</th>
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<tr>
<td>Delay time</td>
<td>424ns (with AD817)</td>
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Table 1: Output voltage fluctuation and delay time from experimental circuit

Remarks — Although we have stated our objective as to speed up the transient response at the voltage regulator end, the same approach is applicable also to the load side. Indeed, there is no compelling reason to limit the application to the regulator end, and the whole essence is to bound voltage fluctuation without excessively large decoupling capacitance.
Figure 10: Experimental results showing transient output voltage (a) without; (b) with $dv/dt$-sense LdCr (scale: 50mV/div, 5ms/div); and (c) blow-up showing delay time (scale: 20mV/div, 200ns/div); voltage from $t_1$ to $t_2$ essentially given by (2), and voltage clamped after $t_2$.

VII. CONCLUSION

The proposed load correction concept represents a new approach to realizing fast transient voltage regulators meeting very tight regulation requirement, yet requiring small decoupling capacitance. The proposed method offers several advantages. Firstly, it is independent of the switching regulator, and hence can be designed and manufactured separately. Secondly, the speed can be arbitrarily fast, and is only limited by device delay. Thirdly, the load corrector dissipates negligible power in the steady state. Finally, practical implementations can be in the form of custom integrated circuits. The various forms of load corrector described in this paper have already been allowed a US patent [7].

REFERENCES


