An Efficient PFC Voltage Regulator With Reduced Redundant Power Processing

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Abstract — Conventional PFC power supplies employ two cascading stages that deal separately with PFC and voltage regulation. Since power is processed serially by two power stages, the efficiency is limited. In this paper a PFC power supply with improved efficiency is proposed. This circuit makes use of a parallel configuration that reduces unnecessary processing of all power by two stages serially. The circuit is derived from consideration of the power flow between the input, the load and the storage capacitor. A specific circuit implementation is described and the test results are reported.

I. INTRODUCTION

Power factor correction (PFC) is becoming an important feature that is compulsorily required of switching power supplies. Conventional approach to designing power supplies with high power factor involves the use of two cascading stages, one responsible for power factor correction and the other for voltage regulation.

Regardless of it being “single stage” in disguise, the power supply essentially contains two power stages [1]–[10]. Since power is processed serially, efficiency is inevitably sacrificed. In Garcia et al. [8], a circuit family is introduced to raise the overall efficiency by permitting part of the power to be processed by only one converter, instead of two. A set of more general configurations is also found in Tse-Chow [11].

In this paper we present yet another circuit configuration of PFC voltage regulator that shows improved efficiency by reducing unnecessary processing of all power by two serially connected stages. Essentially the two stages are connected in such a way that only part of the total power has to be processed by both stages and the rest is allowed to go through only one stage.

II. POWER FLOW REPRESENTATION

In general a voltage regulator with PFC capability must contain an energy storage that buffers the difference between the input power and the load power. A capacitor is typically used as the storage element, and two basic converter stages are needed to convert power from the input to the output, via the storage. A popular design solution

Figure 1: Conventional PFC regulator. (a) Cascade configuration; (b) equivalent power flow representation

is to cascade two stages, with the storage capacitor placed in between, as shown in Fig. 1 (a). As can be seen from the equivalent power flow representation of Fig. 1 (b), input power goes through the two stages serially. Since all power is processed twice, the overall efficiency is given by the product of the efficiencies of the two converter stages, i.e.,

\[ \eta_{\text{cascade}} = \eta_1 \eta_2 \]  

(1)

where \( \eta_1 \) and \( \eta_2 \) are the efficiencies of converters 1 and 2 shown in Fig. 1 (b) respectively.

In fact, for the purpose of achieving PFC and voltage regulation, it is not necessary to process all the input
power by both stages. Intuitively, some part of the input can go directly to the load through one converter stage. Sixteen possible configurations are derived in Tse-Chow [11]. For ease of reference, we reprint these configurations in the Appendix.

Let us now focus on one particular configuration, in which a portion of the input power is converted to the storage, and the rest, after being combined with the storage, is converted directly to the load. The power flow representation of this proposed converter is shown in Fig. 2 (i.e., Type I-IIA shown in Fig. A1 of the Appendix). We may evaluate the theoretical efficiency as follows.

Suppose again that the individual converters' efficiencies are $\eta_1$ and $\eta_2$. Then, the efficiency of this proposed structure can be found as

$$\eta_{\text{overall}} = (1 - m)\eta_1 \eta_2 + m\eta_2$$

$$= \eta_1 \eta_2 + m\eta_2(1 - \eta_1)$$

(2)

where $m$ is the ratio at which power is split at the input, and $m < 1$ [11].

Of course, the improved efficiency remains a theoretical claim since practical efficiency may be affected by such other parameters as component choice, transformer design, use of soft switching, etc. However, even if the efficiency of a converter varies, but within a narrow range (e.g., 0.85 to 0.9), the claim should be quite realistic.

III. DERIVATION OF CIRCUIT TOPOLOGY

Based on the aforementioned power flow representation, we can derive a practical circuit, using a buck-boost converter and a buck converter as converter 1 and converter 2 respectively. The non-isolated realization is shown in Fig. 3 (a). In this circuit, the buck-boost converter converts some part of the input power to the storage capacitor, and the series connection of the input voltage and storage capacitor forms the input for the subsequent buck stage which delivers power to the load.

A practical version of the circuit with transformer isolation is shown in Fig. 3 (b). The reset arrangement for the forward transformer deserves some attention. Specifically the reset loop should avoid going through the mains where rectifiers prohibit current flow in the direction required by the reset. In Fig. 3 (b), the storage capacitor voltage is used to reset the core during off-time of the forward converter.

IV. ANALYSIS OF CIRCUIT OPERATION

The proposed circuit operates in a very simple fashion. In particular we focus on the case where both the buck-boost and the buck converters are operating in continuous mode. This operating mode is suitable for medium to high power applications.

For simplicity, consider the non-isolated version of Fig. 3 (a). We assume that the capacitor voltage is essentially constant, and that the input is a rectified sine function:

$$e(t) = E \sin \omega_m t$$

The input to the buck converter is therefore given by

$$v_{\text{in, buck}} = \frac{P_o}{V_c + E \sin \omega_m t}$$

(4)

where $V_c$ is the capacitor voltage, $\omega_m$ is the mains angular frequency and $E \sin \omega_m t$ is the input voltage. Suppose the output is well regulated by the buck converter. In the steady state, the current drawn by the buck converter is therefore given by

$$i_{\text{in, buck}} = \frac{P_o}{V_c + E \sin \omega_m t}$$

(5)

where $P_o$ is the output power. Thus, as far as the front-end is concerned, we may represent the circuit by the averaged model shown in Fig. 4. Referring to this averaged model, the input current can be expressed as the sum of $d_i i_L$ ($d_i$ being the duty cycle of the buck-boost stage) and the current drawn by the buck stage, i.e.,

$$i_n = d_i i_L + i_{\text{in, buck}}$$

(6)

Now, in order to achieve unity power factor, we attempt to force $i_n$ to follow the input voltage waveform, i.e.,

$$i_n = \frac{1}{E} |E\sin \omega_m t| = \frac{2P_o}{E} |\sin \omega_m t|.$$
Based on the above equations, we can plot the idealized current and voltage waveforms, as illustrated in Fig. 5.

If we attempt to find the inductor current, we will observe a little unpleasant, yet not unacceptable, operating feature of this converter. Since $i_{in,buck} > 0$ for all $t$, we would expect $d_1 i_L$ to take a negative value for some range of $t$ near the zero-crossing of the mains cycle. However, such a requirement cannot be met since, as shown in Fig. 3, a diode is used in the buck-boost stage which prevents $i_L$ from going negative. Thus, this particular realization will have a power factor below one. Nonetheless, as will be shown in the experiment, the power factor of this circuit is still maintained sufficiently high since $i_{in,buck}$ can be reduced by increasing $V_c$.

Remarks — It is possible to achieve unity power factor by replacing the diode of the buck-boost stage with a switch allowing bi-directional current flow, thereby allowing the inductor current to assume a negative value. With suitable control, the input current can thus follow a sine function, even for the region near the zero-crossing of the mains cycle.

V. ANALYSIS OF CONTROL REQUIREMENTS

In order to maintain unity power factor and tight output regulation, the duty cycles of the two stages should vary independently. We denote the duty cycle of the buck-boost stage by $d_1$, and that of the buck stage by $d_2$. Obviously, we can write down $d_2$ almost by inspection:

$$d_2(t) = \frac{U}{V_c + \dot{e} \sin \omega_m t} \tag{8}$$

where $U$ is the dc output voltage. To find $d_1$, we need to solve a set of equations involving $d_1$, $i_L$, and its time derivative. From (5) and (6), we have

$$d_1(t) = \frac{2P_0 \sin \omega_m t}{i_L(t) \dot{e}} - \frac{P_0}{i_L(t)(V_c + \dot{e} \sin \omega_m t)} \tag{9}$$

Also, the inductor equation reads

$$\frac{di_L(t)}{dt} = \frac{(V_c + \dot{e} \sin \omega_m t) d_1(t) - V_c}{L} \tag{10}$$

which can be solved numerically to give $i_L(t)$. Finally, $d_1(t)$ can then be found from (9).

In Fig. 6 we present the MathCad simulated waveforms of the duty cycles and inductor current. Note that the waveforms are missing for regions near the zero-crossings of the mains cycle. This is due to numerical failure in solving the differential equation when $i_L$ approaches zero.

VI. PRACTICAL CONTROL METHODS

In practice, two independent control functions are required to control the buck-boost stage and the forward stage.
1. For the forward stage, we may simply employ a feedback modulation scheme. Moreover, since the input of the forward stage is $V_i + \epsilon \sin \omega_c t$, which can fluctuate quite widely, a feedback scheme may be combined with the feedback modulation to improve the output regulation.

2. In order to achieve power factor correction, the buck-boost converter in the front-end is controlled by the usual current-mode PFC control which effectively forces the input current to follow an input voltage template. Commercial control ICs are available for these purposes, and will be used in constructing the experimental circuit.

VII. EXPERIMENTAL VERIFICATION

The proposed PFC voltage regulator circuit is tested at a power level of 100W and input voltage of 110V (rms). The circuit schematic is shown in Fig. 7. The power factor control employs a standard UC3854 control IC. For output regulation, we use the TL494 control IC, connected in the usual feedback configuration. The measured power factor is 0.997, and the efficiency is 85.5%. The output is regulated at 24V. The input current waveform of the proposed PFC voltage regulator and the input voltage of the forward stage are shown in Fig. 8.

<table>
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<tr>
<th>Parameter</th>
<th>Design value</th>
<th>Measured value</th>
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<tr>
<td>Power</td>
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<td></td>
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<tr>
<td>Input Voltage</td>
<td>110V (rms)</td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>24V</td>
<td>24V (regulated)</td>
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<tr>
<td>Power factor</td>
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<tr>
<td>Overall efficiency</td>
<td>-</td>
<td>85.5%</td>
</tr>
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Table 1: Data and measured results from experimental prototype

VIII. DISCUSSION

A. On Topology

It should not be difficult to see that the circuit reported in this paper is not the only possible circuit that can reduce the amount of redundant processed power. Even for the same configuration used in this paper (Fig. 2), other possibilities exist. For instance, one can employ a flyback converter instead of a forward converter, and end up with a different PFC voltage regulator.

It is yet possible, as mentioned before, to base the design on other configurations with reduced redundant processing power, as shown in Figs. A1 (b) through (p). In fact, some isolated cases have been reported previously in the power electronics literature. For instance, the BIFRED (SEPIC-derived) circuit [1], which belongs to the configuration shown in Fig. A1 (f), has a similar feature in terms of reducing the processing power. In BIFRED, a boost converter and a flyback converter constitute the PFC regulator. The boost stage converts the input power to the load and the storage, while the flyback stage converts power from the storage to the load. Thus, part of the input power can go straight on to the load, without being processed twice.

Another example was demonstrated by García [8]. This circuit has the same power flow configuration as the BIFRED (Fig. A1 (f)), but employs a flyback converter for each of the stages. This circuit was shown to demonstrate improved efficiency.

B. On Control

It is interesting to note that while the BIFRED circuit did not achieve fast output regulation, the García circuit did. Although both circuits share the same configuration (Fig. A1 (f)), they have an essential difference in the control method. The BIFRED is a single-switch converter integrating both stages into a so-called "single-stage", whereas the García circuit has two clearly separated stages allowing independent control of the individual duty cycles. The independent control of two stages has been the key to achieving high pf and fast output regulation simultaneously in this configuration.

IX. CONCLUSION

In this paper we demonstrate how redundant power processing can be reduced or avoided by suitably arranging the basic converter stages that constitute a PFC voltage regulator. The particular circuit described here is based on splitting up the input power into two portions, one being allowed to go straight to the load through only one stage. The result is improved efficiency in comparison with the conventional cascade configuration in which all input power is processed by two converters.

APPENDIX: POWER FLOW CONFIGURATIONS OF PFC REGULATORS

Figure A1 summarizes the sixteen possible configurations of PFC regulators which have been derived from a simple power flow consideration [11]. Of these sixteen configurations, all but Type I-O offer the advantage of reduced redundant power processing, and hence improved efficiency. However, not all of them lead to practical implementations due to limitations in providing isolation, control complexity, etc. These problems are discussed in a separate publication [12].

REFERENCES


Figure 7: Schematic of the experimental circuit

Figure 8: Upper trace: Input voltage to the forward stage 100V/div; Lower trace: Measured input current waveform 500mA/div
Figure A1: Sixteen possible power flow configurations for PFC regulators [11]


