SUBJECT DESCRIPTION FORM

Subject title: VLSI System Design

Subject code: EIE511

Credit value: 3

Responsible staff and department: Dr Bruce C. W. Sham, EIE

Pre-requisite: Nil

Recommended background knowledge: Knowledge of electronic circuit design and microelectronics at a level equivalent to the final year of an honours degree in electronic engineering.

Mutual exclusions: Nil

Learning approach:
Mainly lecture based. Supplement with seminars given by industry managers and engineers, group discussion, and guided laboratory exercises and tutorials.

<table>
<thead>
<tr>
<th>Lecture/Tutorial</th>
<th>27 hours</th>
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<tr>
<td>Practical/Seminar</td>
<td>15 hours</td>
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Assessment:
Continuous Assessment 100%

Objectives:
To provide an understanding of various aspects of VLSI system design. In particular, to look at how different design methodologies and styles are utilized to achieve high-performance, cost-effective integrated circuits.
Knowledge and understanding:

Having successfully completed this module, the student will be able to demonstrate knowledge and understanding of:

- The different design methodologies and styles for CMOS VLSI.
- The design of digital sub-systems with low voltage low power consumption.
- The use of EDA tools in the design process.

Intellectual skills

Having successfully completed the module, the student will be able to:

- Apply top-down, systematic design approach for simple digital CMOS VLSI integrated circuit.
- Derive feasible and efficient testing and design-for-testability structures to achieve high quality and short design turnaround.
- Use hardware description language (VHDL) for hardware modeling to meet performance and time-to-market goals.

Keyword syllabus:

1. Overview
   1.1 Overview of different design methodologies.
   1.2 Design styles (Gate Arrays, Standard Cells, Custom); future technology trends.

2. Semiconductor Technologies
   2.1 Technology comparison - CMOS, BIPOLAR, NMOS, and Bipolar-CMOS.
   2.2 Static and dynamic CMOS circuit design.
   2.3 Basic elements of logic design.

3. Major Design Issues
   3.1 Logic levels, delay calculations, layout and parasitics.
   3.2 Clocking methodologies, clock distribution and driving large load.
   3.3 Layout consideration - importance of good floor-planning and its effect on overall chip performance.
   3.4 Wiring strategies, device scaling, and power estimates; and low power design techniques.
   3.5 Testability: Fault models and fault simulation

4. Digital Design
   4.1 HDL design for arithmetic components: adders and related functions, binary counters, and multipliers.
   4.2 HDL design for real digital systems.

5. Electronic Design Automation
   5.1 Logic Synthesis and floor-planning.
   5.2 Placement and routing.

Indicative reading list and references:


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