# Subject Description Form

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>EIE4111</th>
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<tbody>
<tr>
<td><strong>Subject Title</strong></td>
<td>Advanced VLSI and Computer-Aided Circuit Design</td>
</tr>
<tr>
<td><strong>Credit Value</strong></td>
<td>3</td>
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<tr>
<td><strong>Level</strong></td>
<td>4</td>
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</tbody>
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**Pre-requisite**: Nil*
*remark: It is advisable to take Introduction to VLSI and Computer-Aided Circuit Design (EIE4110). Consult the subject lecturer in case that this course has not been taken before.

**Co-requisite/Exclusion**: Nil

## Objectives

To enable students to gain deeper knowledge and understanding in the following aspects:

1. Complex VLSI circuits and system design include System on Chip (SoC)
2. C-Based VLSI design methodology (High-Level Synthesis)
3. Virtual Platforms using SystemC

## Intended Subject Learning Outcomes

Upon completion of the subject, students will be able to:

**Category A: Professional/academic knowledge and skills**

1. Deepen CMOS VLSI design knowledge
2. Solve problems in system-level and high-level design of CMOS logic circuits, with particular reference increase of productivity
3. Acquire hands-on skills of using High-level synthesis (C-based) CAD tools in VLSI design.
4. Appreciate the design process in VLSI through a mini-project on the design of a Configurable System on Chip (CSoC)

**Category B: Attributes for all-roundedness**

5. Communicate effectively.
6. Think critically and creatively.
7. Assimilate new technological and development in related field.

## Subject Synopsis/Indicative Syllabus

### Syllabus:

1. **High-Level Synthesis**
   VLSI design using high-level programming languages (ANSI-C, SystemC).
   Different scheduling modes (manual, automatic, pipelined)

2. **Simulation models**
   Behavioural simulation, cycle-accurate simulation, RTL simulation, gate-netlist simulation. Trade-offs and applicability

3. **Design Space Exploration**
   Automatic generation of HW architectures with different area vs. performance trade-offs from the same C/SystemC program

4. **System-level VLSI Design**
   Virtual Platforms, Transaction-level Models (TLM)

5. **SystemC**
   C++ class to model the behaviour of VLSI circuits

6. **Configurable SoCs**
   Embedded SW and Programmable Logic design flow.
Laboratory Experiment:

1. Practice of CAD tools for VLSI design: high-level synthesis (HLS), C/SystemC based VLSI design
2. Use Programmable SoC devices (e.g. Xilinx Zynq) to build complete SoCs (embedded SW-ARM processor and HW-FPGA)
3. Mini-project: design of a system for computer or communication applications and prototype if on a configurable SoC.

<table>
<thead>
<tr>
<th>Teaching/ Learning Methodology</th>
<th>Teaching and Learning Method</th>
<th>Intended Subject Learning Outcome</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lectures, supplemented with interactive questions and answers, and short quizzes</td>
<td>1, 2, 6, 7</td>
<td>In lectures, students are introduced to the knowledge of the subject, and comprehension is strengthened with interactive Q&amp;A and short quizzes. They will be able to explain and generalize knowledge in VLSI.</td>
<td></td>
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<tr>
<td>Tutorials where design problems are discussed, and are given to students for them to solve</td>
<td>1, 2, 5, 6</td>
<td>In tutorials, students apply what they have learnt in analyzing the cases and solving the problems given by the tutor. They will analyze the given information, compare and contrast different scenarios and propose solutions or alternatives.</td>
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<tr>
<td>Laboratory sessions, where students will perform a mini-project on a subsystem design using CAD tools. They will have to write a report on their mini-projects.</td>
<td>2, 3, 4, 5, 6</td>
<td>Students acquire hands-on experience in using CAD tools in VLSI design, and apply what they have learnt in lectures/tutorials to do a mini-project on the design of a sub-system.</td>
<td></td>
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<tr>
<td>Assignment and Homework</td>
<td>1, 2, 3, 4, 5, 6</td>
<td>Through working assignment and homework, students will develop a firm understanding and comprehension of the knowledge taught. They will analyze given information and apply knowledge in solving problem. For some design type of questions, they will have to synthesize solutions by evaluating different alternatives.</td>
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Assessment Methods in Alignment with Intended Subject Learning Outcomes

<table>
<thead>
<tr>
<th>Specific Assessment Methods/Tasks</th>
<th>% Weighting</th>
<th>Intended Subject Learning Outcomes to be Assessed (Please tick as appropriate)</th>
</tr>
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<tbody>
<tr>
<td>1. Continuous Assessment (total 50%)</td>
<td>40%</td>
<td>1 2 3 4 5 6 7</td>
</tr>
<tr>
<td>• Min-project</td>
<td>✓ ✓ ✓ ✓ ✓ ✓</td>
<td></td>
</tr>
<tr>
<td>• Laboratory works and reports</td>
<td>10%</td>
<td>✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td>2. Examination</td>
<td>50%</td>
<td>✓ ✓ ✓ ✓ ✓</td>
</tr>
<tr>
<td>Total</td>
<td>100%</td>
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</table>
The continuous assessment will consist of a mini-project, a number of laboratory sessions.

**Explanation of the appropriateness of the assessment methods in assessing the intended learning outcomes:**

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<tr>
<td>Mini-project</td>
<td>Students are required to conduct one mini-project in teams of 3-4 students. The emphasis is on assessing their ability to apply knowledge and skills learned in designing a complex VLSI system, ability in working with other people and ability to take data and relate the measurement results to theory. Expectation and grading criteria will be given.</td>
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<tr>
<td>Laboratory works and reports</td>
<td>Students will be required to perform 5-6 laboratory sessions and write an individual laboratory report. The emphasis is on assessing their ability to use VLSI CAD tools effectively to perform VLSI design. Expectation and grading criteria will be given as in the case of mini-project.</td>
</tr>
<tr>
<td>End-of-semester test and Examination</td>
<td>There will be an end-of-semester examination to assess students’ achievement of all the learning outcomes. Expectation and grading criteria will be given as in the case of mini-project.</td>
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**Student Study Effort Expected**

**Class contact (time-tabled):**

- Lecture: 24 Hours
- Tutorial/Laboratory/Practice Classes: 15 Hours

**Other student study effort:**

- Lecture: preview/review of notes; homework/assignment; preparation for test/quizzes/examination: 36 Hours
- Tutorial/Laboratory/Practice Classes: preview of materials, revision and/or reports writing: 30 Hours

**Total student study effort:** 105 Hours

**Reading List and References**

**Reference Books:**


**Last Updated**

March 2014

**Prepared by**

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