1×4 all-optical packet switch with all-optical header processing

L. F. K. Lui,1 Lixin Xu,1,2 P. K. A. Wai,1 L. Y. Chan,1 C. C. Lee,1 H. Y. Tam,3 and M. S. Demokan3

1Photonics Research Centre and Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Hung Hom, Hong Kong
Phone: +852 2766-6231, fax: +852 2362-8439, email: enwai@polyu.edu.hk
2Department of Physics, University of Science and Technology of China, Hefei, 230026, China
3Photonics Research Centre and Department of Electrical Engineering, The Hong Kong Polytechnic University, Hung Hom, Hong Kong

Abstract: We demonstrated a 1×4 all-optical packet switch using injection-locking in a Fabry-Perot laser diode for all-optical header processing and cross gain modulation in an SOA for packet switching.

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1. Introduction

Recently, by utilizing the bistability and multi-wavelength injection-locking properties of Fabry-Perot laser diodes (FP-LD), we demonstrated all-optical packet switching with all-optical header processing at 10 Gb/s using a single FP-LD [1]. We used a self-routing address in which each output port of every node in a network is identified by the location of a single bit in the address header [2]. The FP-LD blocked a data packet if its header bit matches temporally with a ‘1’ bit in a special two-level control packet. However, because of the finite response time of the FP-LD, part of the address bits of the blocked packets are able to pass through before injection-locking by the control packets can take place (Fig. 1a) thus limiting the cascadability of the proposed all-optical packet switches. The small locking range of the FP-LD (~0.25 nm) also limits the maximum data rate the switch can operate. In this work, we proposed and demonstrated all-optical processing of the packet headers and control packet generation using a FP-LD [3]. The switched control packets from the FP-LD are then used for all-optical packet switching by cross gain modulation in a semiconductor optical amplifier (SOA). With the two-stage switching process, the packets are blocked without part of their address bit slipping through. The quality of the switched packets also improves.

2. Operating principle

Figure 1b shows a schematic of the proposed 1×N all-optical packet switch. An incoming packet is first split into N parts using a 1×N coupler. At each output port, the data signal is further split into two parts. One part is injected into the all-optical header processor (AOHP) which will generate a control signal if the header of the packet does not match the address of the output port encoded in a local control packet. The switched control signal from the AOHP is then combined with the other parts of the data signal and injected into the all-optical shutter (AOS) which will transmit the data packet if the control signal is low.

The AOHP performs both all-optical header processing and control packet switching using a single Fabry-Perot laser diode (FP-LD) [3]. In the address, we indicate the intended output port of a packet at a node by setting the corresponding header bit to ‘0’ and the rest of the header bits to ‘1’s [2]. The special two-level control packet header encodes the complement of the address of the output port to which the AOHP is attached. Figure 2a shows two data packets with address headers ‘0111’ and ‘1011’ intending for output port 1 and 2 respectively. Figure 2b
shows the local control packets at output port 2 with the address ‘0100’. In the AOHP, if the ‘1’ bit in the control packet header coincide with a ‘1’ bit in the data packet header, the control packet will injection-lock the FP-LD at \(\lambda_c\) and maintain injection locking until the end of the control packet [1]. The output of the FP-LD at \(\lambda_c\) will be high in this case and low otherwise (Fig. 2c). The switched control signal at the output of the AOHP at \(\lambda_c\) is then combined synchronously with the original data signal in an SOA which is set to transmit a data packet at \(\lambda_d\) if the control packet at \(\lambda_c\) is low.

3. Experimental results

Figure 3 shows the experimental setup. For the AOHP, the control packets at 1540.16 nm are generated using a 10 Gb/s NRZ pulse pattern generator, a 155 MHz pulse pattern generator, and two 10 Gb/s LiNbO\(_3\) modulators on the output of a tunable laser (TL_1). The injected power is 5.9 dBm and the wavelength detune is +0.22 nm. The output of the 155 MHz pulse pattern generator is triggered by the clock/32 output of the 10 Gb/s pulse pattern generator for synchronization. The 10 Gb/s data packets at 1542.76 nm are generated by externally modulating another tunable laser (TL_3) using another 10 Gb/s non-return-to-zero (NRZ) pulse pattern generator and a LiNbO\(_3\) modulator. The injected power is -6.9 dBm and the wavelength detune is -0.01 nm. The two 10 Gb/s pattern generators are synchronized using an external 10 GHz clock. The cw stabilizer signal at 1537.13 nm is generated by a third tunable laser (TL_2) with an injected power of -11 dBm and the wavelength detune is +0.02 nm. The bias current of the FP-LD is 2.0 I\(_{th}\) where I\(_{th}\) is the threshold current. The data packet header is 4-bit long corresponding to a 1×4 switch. The bit period at the header is 200 ps long for a header rate of 5 Gb/s. The input data signals consist of packets with headers ‘0111’, ‘1011’, ‘1101’, and ‘1110’ for pk_1 to pk_4 respectively. The data packet payload is 48 bits long. The payload rate is 10 Gb/s and the guard period is 800 ps. The header of the control packet is ‘0100’ corresponding to output port 2. Figures 4a, 4b, and 4c respectively show the synchronized timing diagrams of four consecutive data packets, two-level control packets, data packet headers and control packet headers at the input of the AOHP. Figure 4d shows the switched control packets at the output of the AOHP. Figures 5a and 5b show the timing diagrams of the data packets and control packets at the input of the AOS. Figures 5c and 5d show the switched output of the data signal at 3 ns/div and 1 ns/div respectively. We observed that pk_2 is successfully switched out and the data is not distorted by the switching action. Also, no part of the address bits from the other three packets is transmitted.

4. Conclusion

In conclusion, we have demonstrated all-optical processing of the packet header and control packet generation using a single FP-LD. The switched control signals are then used for all-optical packet switching by cross gain modulation in an SOA. The header rate is 5 G/s and the payload rate is 10 Gb/s. Packets are blocked without parts of their address bits slipping through. The quality of the switched packets also significantly improves compared to that in [1].

5. References

Fig. 1. (a) Residual address bits (enclosed by dashed circles) from blocked packets in all-optical packet switch proposed in [1]. (b) The proposed 1×N all-optical switch. Note: AOHP – All-Optical Header Processor, AOS – All-Optical Shutter, COUP – coupler.

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a. data packet ($\lambda_d$) at the input of the AOHP

b. control packet ($\lambda_c$) at the input of the AOHP
c. output of AOHP at $\lambda_c$
   - injection-locked
   - NOT injection-locked

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Fig. 2. The time domain switching mechanism in the all-optical header processor.

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AOHP

Fig. 3. Experimental setup. Note: TL – tunable laser; FP-LD – Fabry-Perot laser diode; SOA – semiconductor optical amplifier; EDFA – erbium-doped fiber amplifier; TBPF – tunable bandpass filter; ODL – variable optical delay line; PC – polarization controller; AOHP – All-Optical Header Processor, AOS – All-Optical Shutter

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Fig. 4 Synchronized timing diagrams of the signals at the AOHP: (a) input data packets, (b) input control signals, (c) aligned header of the input packets and input control signal, and (d) switched control signal at the AOHP output.

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Fig. 5 Synchronized timing diagrams for the signals at the AOS: (a) input data packets; (b) input control packet (output from the AOHP); (c) switched data packet at the output of the AOS; and (d) zoom-in switched data packet at the output of the AOS.