All-optical packet switching of 160 Gb/s packets with all-optical processing of 10 Gb/s headers

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Abstract: We report the first demonstration of all-optical packet switching of 160 Gb/s packets with all-optical header processing of the 10 Gb/s packet headers. The timing diagrams before and after packet switching are shown.

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1. Introduction
High speed all-optical packet switching best suits the bursty nature of the multimedia traffic in future optical communication systems because of the elimination of the opto-electronic conversion. Most of the research on optical packet switching to date focuses on hybrid electro-optical packet switching [1]. A 1×2 optical packet switch with all-optical header processing was implemented using a SLALOM structure and an optical flip-flop memory [2]. The data rate of the packet payload is 2.5 Gb/s. Recently, we demonstrated all-optical packet switching with all-optical header processing using multi-wavelength injection locking and bistability properties in Fabry-Perot laser diodes (FP-LD) [3]. The header rate and payload data rate are both 10 Gb/s. In this paper, we demonstrated all-optical packet switching of 160 Gb/s packets with on-the-fly all-optical header processing of the 10 Gb/s headers. The 160 Gb/s payload is switched on or off using a semiconductor optical amplifier (SOA) based on the processing of a single bit in the 10 Gb/s data packet header by a FP-LD. The all-optical packet switch demonstrated here can be used to realize the packet-drop function in the all-optical packet-switched ring network proposed in [4].

2. Design of the all-optical packet switch
Figure 1 shows a schematic of the proposed all-optical packet on/off switch. An incoming packet at wavelength $\lambda_d$ is first split into two parts. One part is injected into a header extractor (HE) which extracts the 10 Gb/s header from the 160 Gb/s payload. It is then passed through an all-optical header processor (AOHP) together with a locally generated control signal with wavelength $\lambda_c$. We used a self routing address in which a data packet identifies its intended output port at a node by setting the corresponding header bit to ‘1’ and the rest of the header bits to ‘0’ [5]. A special two-level control signal header encodes the address of the output port to which the AOHP is attached. At the AOHP, if the ‘1’ bit in the control signal header coincides with a ‘1’ bit in the data packet header, the control signal will injection-lock the FP-LD at $\lambda_c$ and maintain injection locking until the end of the control signal [3]. The switched control signal at the output of the AOHP at $\lambda_c$ is then combined synchronously with the original data packets in an all-optical on/off switch (AOS) which is set to transmit a data packet at $\lambda_d$ if the switched control signal at $\lambda_c$ is low and vice versa.

3. Experimental Setup and results
Figure 2 shows the experimental setup of the all-optical packet switch. We generated the 160 Gb/s packets by first multiplexing the 10 Gb/s output from a tunable mode-locked laser (TMLL) which has a pulse width of ~1.7 ps. We then modulated the resulting 160 Gb/s bit stream using a 10 Gb/s non-return-to-zero (NRZ) pulse pattern generator and a LiNbO$_3$ modulator. We encoded four types of packets with header addresses ‘1000’, ‘0100’, ‘0010’ and
‘0001’ for pk-1, pk-2, pk-3, and pk-4 respectively. The payload of all four types of packets is set to all ‘1’s. Consequently, the effective data rate of the packet header is only 10 Gb/s while the payload data rate remains at 160 Gb/s. Since the bandwidth of the 160 Gb/s data signal is significantly larger than the typical locking range of FP-LDs, the data spectrum must be filtered down before header processing. We used a DC biased 10 Gb/s electro-absorption modulator (EAM) as a low pass filter – because of the slow response time in the wavelength conversion process – which converts the 16 RZ-formatted ‘1’ bits in the header into a single ‘1’ bit at 10 Gb/s. The extracted 10 Gb/s headers at wavelength, power, and detune of 1554.87 nm, −15.9 dBm, and −0.05 nm respectively are then injected into a FP-LD together with a local control signal and a CW stabilizer signal for header processing. The two-level control signal at wavelength 1558.45 nm (λc) is generated using a two pulse pattern generators, and two LiNbO3 modulators on the output of a tunable laser (TL-3) with injected power of −6.9 dBm and wavelength detune of +0.17 nm. The header of the control signal contains the pattern ‘0010’ which is the address of pk-3. The wavelength, injected power, and detune of the CW stabilizer signal are 1553.39 nm, −15.7 dBm, and +0.01 nm respectively. The input power of the control signal is sufficiently strong such that the FP-LD emits at λc irrespective whether the FP-LD is injection-locked at λc but the FP-LD output at λc in these two cases have different states of polarization. We used a filter and a polarizer to obtain the output at λc when the FP-LD is not injection-locked at λc. This switched control signal is then injected into an SOA with the other portion of the data signal.

Figures 3a to 3f show the synchronized timing diagrams of the optical signals during header processing: (a) the 160 Gb/s input data packets at 6 ns/div, (b) the zoom-in 160 Gb/s input data packets at 10 ps/div, (c) the extracted headers of the input data, (d) the zoom-in data and control signal headers at 500 ps/div, (e) the input control signal, (f) the switched control signal, (g) the switched data packets after the SOA; and (h) the zoom-in of the switched 160 Gb/s data payload.

3. Conclusion

We demonstrated all-optical packet switching of 160 Gb/s packets with all-optical processing of header at 10 Gb/s. The all-optical packet switch is constructed using a FP-LD, an EAM, and an SOA. The data is switched successfully.

4. References