# IC Engineering

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References:

1. Richard C. Jaeger, Introduction to Microelectronic Fabrication, Prentice Hall
2. Neil Weste, Kamran Eshraghian, Principles of CMOS VLSI Design, Addison-Wesley
3. S. M. Sze, VLSI Technology, McGraw Hill



## Learning outcomes:

**Academic knowledge and skills:**

- Understand the fundamentals of VLSI and associated technologies
- Understand the physical mechanism of IC fabrication processes
- Solve problems in basic CMOS logic circuits
- Acquire hands-on skills of using CAD tools in VLSI design

**Attributes for all-roundness:**

- Communicate effectively
- Think critically and creatively
- Assimilate new technological and development in related field

**CONTENTS:**

1. Development of ICs
2. Bipolar integrated circuits
3. MOSFET Physics
4. MOS integrated circuits
5. Design of Integrated Circuits
6. Incorporation and Diffusion of Impurities
7. Thermal oxidation
8. Chemical vapour deposition
9. Metallization
10. Photolithography



## 1. Development of Integrated Circuits

• The advent of revolution in electronics made possible by the development of higher integration of density of **silicon** integrated circuits, e.g. memories of 512M

• Advantages of increased density of integration:
- reducing system cost (IC cost mainly in packages),
- enhancing overall system function, and
- increasing reliability.

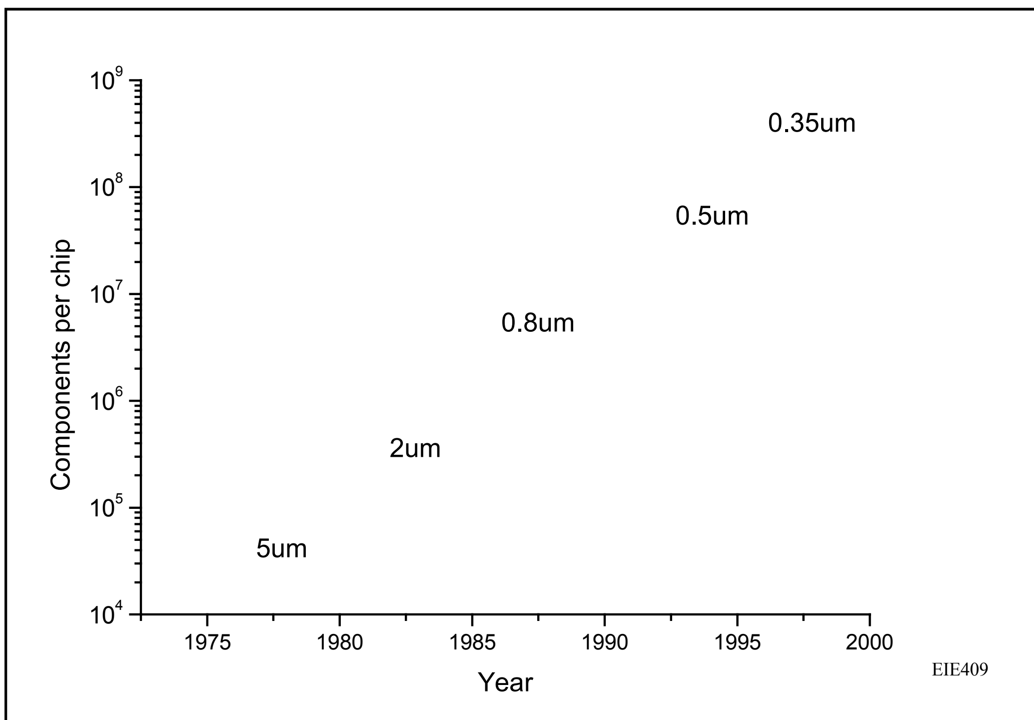
• Requires tremendous research in several areas: **semiconductor device physics, fabrication technology and computer-aided-design tools.**

• Increasing integration density on the wafer is achieved by **shrinking the dimensions** of the semiconductor device. Small geometry transistors also have much faster **speed**.

• In MOS IC, the channel length of the MOSFET has been continuously decreased from an initial value of 10 µm to deep sub-micron (0.18µm) in the present manufacturing state of the art. In research labs, devices based on nanotechnology (65 nm and less) are built.

• Must understand clearly the physics of small geometry devices in order to design MOSFET in VLSI, which are very different from long channel devices.





• To fabricate small geometry devices requires the definition of very fine patterns on the wafer during the photolithographic process. Other physical problems in small size structures urges the development of new **fabrication process**, such as photolithography, plasma etching .

• The fabrication environment has also become more stringent because of the yield problem in large area wafers. Class 10 or even lower clean room has to be used to control the amount of dust particles.



• Finally given the capability to fabricate high density integrated circuits, we must be able to design the circuit itself starting from the system specifications. The design of a circuit with millions of transistors (including logic, circuit and mask layout design) is only possible with the use of **computer-aided-design tools** on workstations. This is an area where computer science plays an important role in the development of integrated circuits.

**Hierarchies of Design**

• System level – digital (e.g. PCs), mixed-signal (digital & analogue, e.g. mobile phone)
• Circuit level – logic circuits, analog circuits
• Device & process level – semiconductor device & fabrication

## 1.1 Monolithic Integrated Circuits

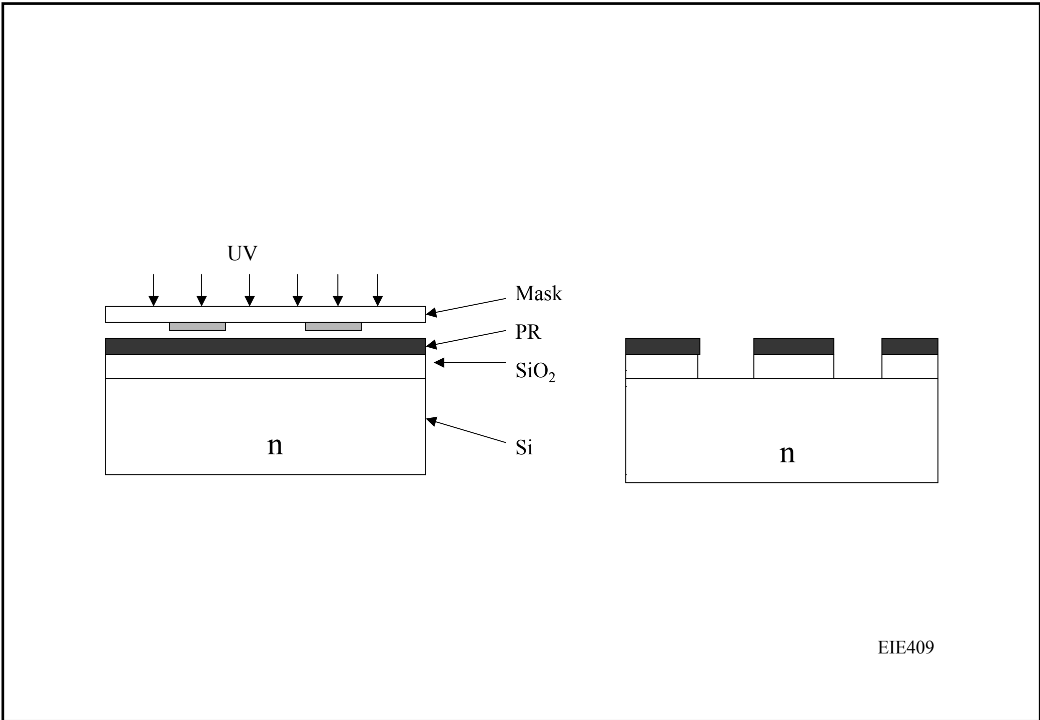
• Circuits that are placed entirely on a single chip of semiconductor (usually Si) are called **monolithic** integrated circuits. Monolithic circuits have the advantage that mass production by batch processing is possible. Many identical circuits are fabricated simultaneously on a Si wafer (up to 12" diameter), which is then sawed into many chips. Each chip is finally enclosed in plastic or ceramic packages to become an IC.



## 1.2 Fabrication of monolithic circuits: simple review

• The basic idea behind the fabrication process is to selectively dope certain regions of the semiconductor to form p-n junctions, and then interconnect the doped regions to form devices and circuits.

• Since $SiO_2$ is a good barrier to most dopant impurities, **selective doping** is done through windows opened in a thermal grown oxide layer using **photolithographic** techniques. By exposing the photoresist coated on the wafer through a glass mask to UV light, the desired pattern can be developed on the photoresist, and then transferred to the oxide layer.


UV
Mask
PR
SiO2
Si
n
n
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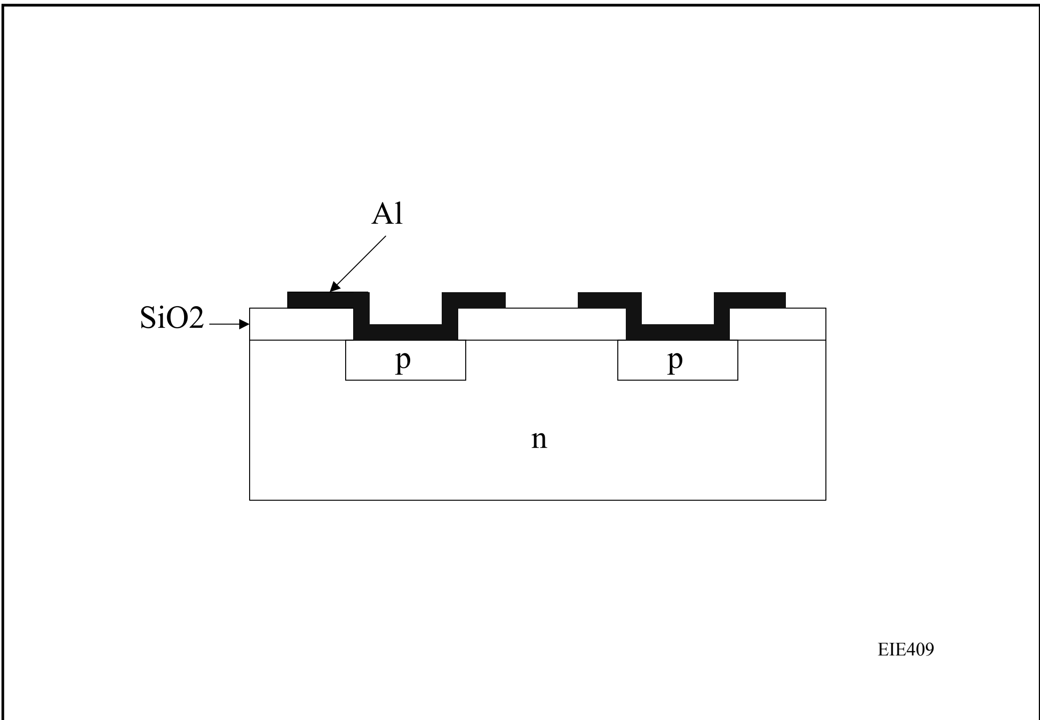
Al
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p
p
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Main **fabrication processes** include:

i) Thermal **oxidation** (field oxide, and gate oxide in MOSFET),

ii) diffusion, ion implantation for **doping** impurities,

iii) **photolithographic** process for defining pattern,

iv) **etching** of insulator, metal, or Si by chemical solution or plasma,

v) deposition of polycrystalline Si , silicon oxide, silicon nitride by **chemical vapour deposition** (CVD),

vi) deposition of **metallization** layer by physical vapour deposition for Al, and electroplating for Cu.



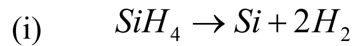
• Impurities can be doped into a semiconductor to form a p-n junction by thermal diffusion and ion implantation. Incorporation of dopant impurities in selected regions can be carried out through windows in a $SiO_2$ masking layer.

• Common dopant impurities in Si:
p type acceptors – boron; n type donors – phosphorus, arsenic

• Dopant incorporation by **diffusion** takes place at high temperatures ~1000°C in a furnace. **Ion implantation** is particularly useful in forming shallow junctions with high doping concentrations. Ionized-projectile atoms are introduced into solid targets with enough kinetic energy (3 to 500keV) to penetrate beyond the surface regions.

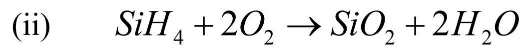
• **Chemical vapour deposition** forms a thin layer of material on wafer surface by reaction of gases passed into a furnace at high temperatures.

Applications:

(i) 

$$SiH_4 \rightarrow Si + 2H_2$$

produces polycrystalline Si layer used as the gate electrode of MOSFETs.

(ii) 

$$SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O$$

produces silicon dioxide layer, used for insulation between multi-level metal layers