

Literature Review Report 2

Overview of Power Factor Correction

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Abstract

In this report, we will review the fundamentals of power factor correction. We will also introduce a power factor corrector using the most popular topology, the boost PFC pre-regulator. Then a simulation model of a boost PFC pre-regulator by Dranga and Tse[3], together with some experimental verification result will also be presented.

1 Introduction

The power factor correction and the reduction of the line harmonics becomes more and more important as the amount of line-fed electronic equipment grows and the international regulation requirements are tightened.

For many line-fed equipments, such as the AC/DC switching mode power supply, the input rectifier frontend draws narrow pulsating currents from the AC line only at the peak of the supply voltage. The current pulses contain large-amplitude harmonics and produce many undesirable effect on the AC line. They will cause additional transformer and distribution loss, which will be dissipated in the transformer and distribution line as heat, which is a sort of energy wastage. Moreover, the odd harmonic components result in a compensating current flow in the neutral line of a three-phase, four-wire distribution system and produce clipping in AC line voltage.

Besides, many countries have proposed and tightened regulations to further cut down such power line pollution. The regulation IEC1000-3-2, which in 1998 was a generally accepted standard to set the limit of line harmonics produced by different categories or classes of electronic equipments.

The above reasons make power factor correction become a "evergreen" research topics no matter in academic or industries over so many years. Different kinds of innovative topologies and control methods have been introduced to further improve the performance in harmonics reductions, efficiency and stability.

This literature review report mainly gives an overview on some fundamental concepts of power factor correction. First of all, the definition of power factor will be given and we will discuss the common power factor problem in single stage switching mode power supply. Then the passive and active power factor correction will be introduced, in which we will review some basic topologies of PFC corrector. Following this we will go through some common active current control schemes currently used in industry. To give more details, the stability analysis and the bifurcation behavior in PFC are also discussed. A boost PFC simulation model is presented following with the experimental verification to identify the stability boundaries with different circuit parameters. In the last session, a conclusion will be given as well as the future plan of research work to follow up the related issue.

2 Definition of Power Factor

In terms of strictly passive reactive load, power factor is defined as the cosine of the phase angle θ between the voltage and current waveform. For an rms input voltage V_{rms} and rms input current I_{rms} , the total power taken from the line is $V_{rms}I_{rms}$, which is referred as "apparent power". But the actual power consumed by the load is only $V_{rms}I_{rms}\cos\theta$. It means only the component of input current which is in phase with the voltage across the load resistance $I_{rms}\cos\theta$ contributes to the load. This actual power is also referred as "real power". This brings an alternative way to express power factor as a ratio of real power to apparent power.

$$Power\ factor = \frac{Real\ power}{Apparent\ power} \quad (1)$$

$$= \frac{V_{rms}I_{rms}\cos\theta}{V_{rms}I_{rms}} \quad (2)$$

$$= \cos\theta \quad (3)$$

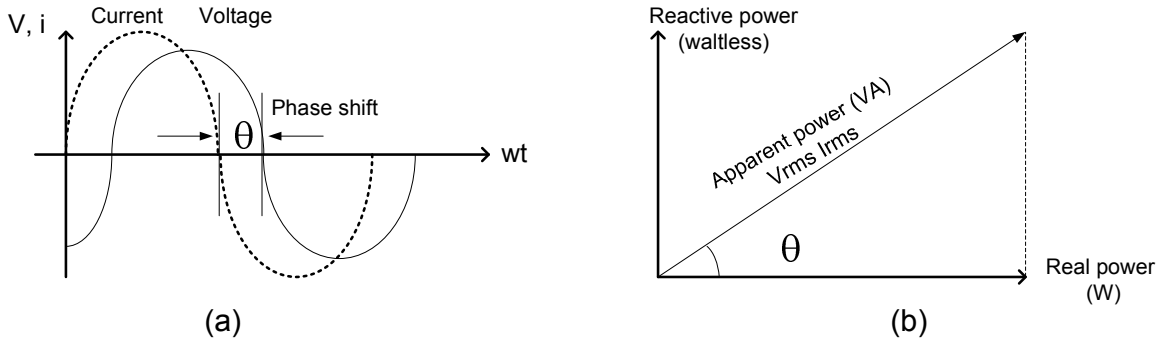


Figure 1: (a) Line voltage and current at the input of a reactive load. (b) Vector diagram showing the apparent power exceed the resistive and reactive power

However, the above stated definition is only valid on condition that both the input current and input voltage are ideal sinusoidal waveform, which is not the case in most real-world power supplies.

When the input current or input voltage is non-sinusoidal, power factor consists of two factors:

1. The displacement factor measures the phase angle, PF_{disp}
2. The distortion factor measures the waveform shape, PF_{dist}

As mentioned before,

$$PF_{disp} = \cos\theta \quad (4)$$

while

$$PF_{dist} = \frac{1}{\sqrt{(1 + THD^2)}} \quad (5)$$

$$= \frac{1}{\sqrt{1 + (I_2/I_1)^2 + (I_3/I_1)^2 + (I_i/I_1)^2 + \dots}} \quad (6)$$

Where THD stands for "Total harmonic distortion" I_i is the rms of the i th harmonic input current.

And the extended power factor definition becomes:

$$\text{Power factor} = PF_{disp}PF_{dist} \quad (7)$$

$$= \frac{\cos\theta}{\sqrt{1 + THD^2}} \quad (8)$$

Power factor is a useful measurement of power quality. It can vary between 0 and 1. when the current and voltage waveforms are in phase and of ideal sinusoidal shape, the power factor is 1 (unity). However, Redl [2] pointed out the truth that high power factor (close to 1) can still be obtained even with high current distortion. The purpose of making the power factor equal to unity is to make the circuit look purely resistive (apparent power equals to real power).

3 Power Factor Problem in Switching Mode Power Supply

In switching mode power supplies, the problem lies in the input rectification and filter network. As we all know, the rectifiers can only conduct current when the ac line voltage exceeds the voltage across the input filter capacitor. With the large bulk capacitor right after the bridge rectifier, this conduction only occurs near the peak of the ac voltage. It results in large input current spike, which is much higher than the expected average input current. Due to the rectifier's discontinuous conduction, the input lines is rich in odd harmonics and leads to distortion of the ac voltage waveform. The highly distorted input current results in low power factor. Besides, as no current is drawn when the rectifiers are not conducting, thus flowing away a significant portion of power system's energy capability

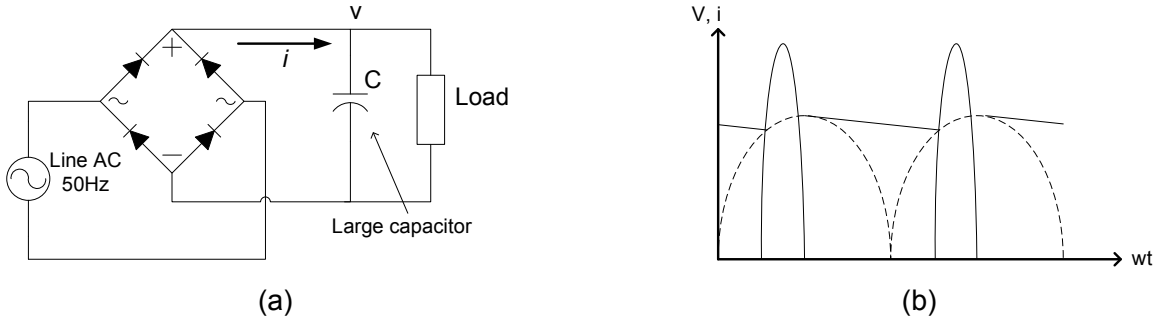


Figure 2: (a) A typical rectifier input stage with large input capacitor for a direct off-line switching mode power supply. (b) Rectifier output voltage and current with large input filter capacitor

4 Passive Power Factor Correction

Power factor can be improved by using either passive power factor correction or active power factor correction. To be brief, passive power factor correction involves the use of linear inductors and capacitors to filter or minimize the harmonic components and improve the power factor. For example, the passive LCR input filter is typically used in passive PFC electronic ballasts for harmonic reduction, or the rectifier with filter inductor as shown in Fig 3. According to Kelley and Yadusky, 1989 [4], if the inductor and capacitor value are properly selected, the power factor can reach up to 90.5 percentage even with small inductor and capacitor. Other examples are the "valley-fill" power factor correction circuit described by Spangler in 1988 [5] and then later comes its improved version by KitSum [6]. In general, passive solutions offer reliable, rugged and 'quiet' reduction of harmonic currents. They are insensitive to line surges and spikes. However, they also have

many disadvantages: They are relatively bulky. Also they are sensitive to line frequency and may produce excessive phase shift. Moreover, they lack voltage regulation and the dynamic response is poor.

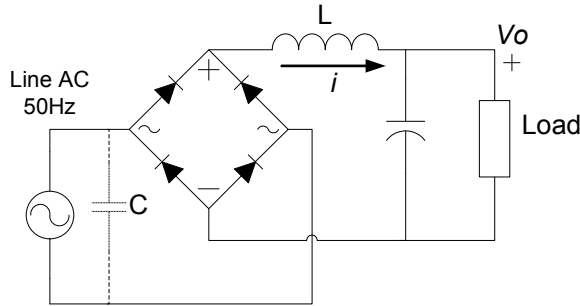


Figure 3: The rectifier with filter inductor

5 Active Power Factor Correction

Active power factor correction uses controlled switches to force the line current to follow the envelope of the line voltage and go in phase with it. Active power factor correction circuits can employ non-isolated switching power supply topologies, such as buck, boost and buck/boost.

5.1 The buck corrector

The buck topology produces an dc output voltage lower than its input voltage. This can present a problem when the instantaneous line voltage is below the output voltage. There will be no line current and lead to significant line-current distortion. Also, the switch rms current and the differential-mode EMI current are high. The buck PFC corrector is shown in Fig 4.

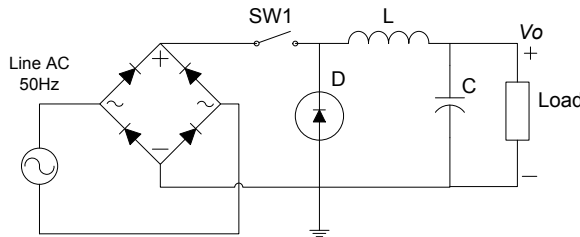


Figure 4: The buck PFC corrector

5.2 The buck-boost corrector

Buck-boost topology produces a negative output voltage with respect to input ground. It is able to achieve low line-current distortion while maintaining overload protection and voltage step-down capability. The major disadvantages includes the inverted output, the high-side power switch, which is difficult to drive and the higher voltage stress for the power switch and the free-wheeling diode. A two-switch buck-boost corrector is described by R. Redl [2] to eliminate some of the disadvantages such as the inverted output and the increased voltage stress. The cost are the additional power switch and diode. By different on and off combination of the two switches, the converter can work as a buck, boost or buck/boost corrector depends on

requirement. For example, keeping S1 ON and only operates S1 turn the corrector into boost mode, which can be used to increase efficiency during heavy load condition. While buck mode (keeping S2 open and only operates S1) is used intermittently during start-up. The buck-boost PFC corrector and its two-switches version are shown in Fig. 5 and Fig 6 respectively.

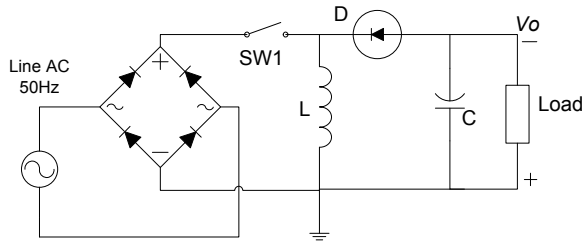


Figure 5: The buck-boost PFC corrector

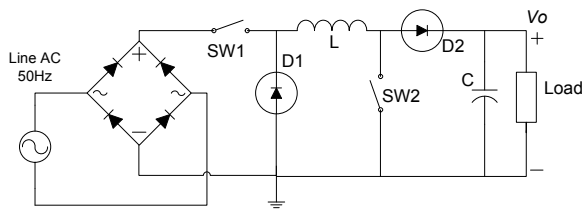


Figure 6: The two-switch buck-boost PFC corrector

5.3 The boost corrector

The Boost is the most popular topology. It has a low-side power switch which is easy to drive and the circuit is simple to implement. Also, as the input current is continuous, it produces the lowest level of conducted noise and the best input current waveform. The disadvantages is the high output voltage produced by the boost topology. The output voltage must be greater than the highest peak of the input voltage for the PWM to function properly. As there is no switch between the line and the output, there's no inrush current limiting, overload or short-circuit protection. Moreover over-voltage protection for the load is not available. The boost PFC corrector is shown in Fig 7. There are many variation of the boost corrector, with different number of switches, diodes and storage capacitor and the location of the inductor. For example, the single-switch boost corrector variation from Sreiber, 1991 [7] and the two-switch boost corrector variation from Mitchell, 1983 [8], which are shown in Fig 8 and Fig 9 respectively.

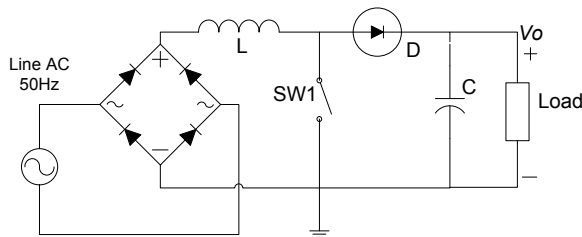


Figure 7: The boost PFC corrector

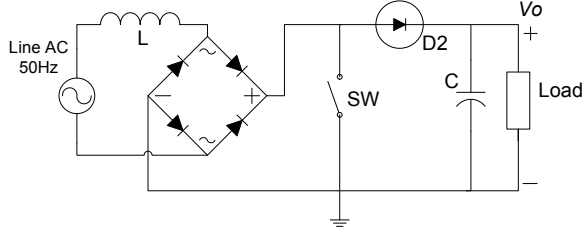


Figure 8: The single-switch boost corrector variation from Sreiber, 1991

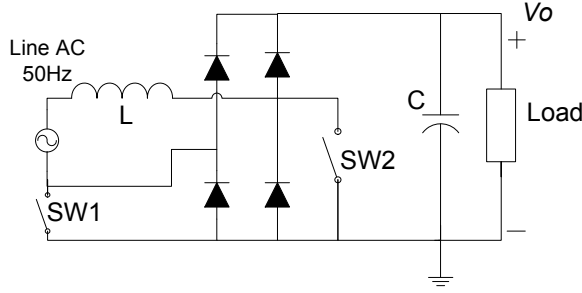


Figure 9: The two-switch boost corrector variation from Mitchell, 1983

5.4 The quasi-resonant and interleaved corrector

Besides square-wave converter topologies, PFC can also be achieved by using quasi-resonant and interleaved converters, which can reduce the switching loss with zero-current switching (ZCS) and zero-voltage switching (ZVS). Examples are the Cuk power factor corrector and the SEPIC corrector. Besides the non-isolated correctors, isolated power factor corrector can be achieved by using transformer-coupled version of the basic converter, for example, the flyback corrector is the isolated version of the buck-boost corrector.

5.5 Rules for PFC topologies

So far quite a large number of PFC topologies have been discovered, but they are reported as separated case of innovations. Tse ,2002 [9] derived the basic requirement for the PFC topology based on zero order networks and duality theories, which defined the zero order converter and suggested that a converter topology can be used for power factor correction if its input impedance is of zero order(resistive). Also, some rules to identify the zero order input impedance of a converter is also presented. Based on the theories derived, it can be easily explained that the buck-boost converter operating in DCM is a natural PFC as the input impedance is zero-order if certain circuit parameters , d^2T , is kept constant.

$$R_{in,buck-boost} = \frac{2L}{d^2T} \quad (9)$$

Although buck-boost corrector is perfect for power factor correction due to its low current distortion, it exhibits a higher peak current stress in the switching components and yields a lower efficiency. Boost converter thus become a more favorable choice based on the overall performance and we will go into detail in later sessions.

6 Active Control of Line Current

Active control of line current means forcing or programming the input current to follow the envelope of the sinusoidal input voltage waveform. We will introduce several common control methods with controller ICs available in the industry. The general active current control scheme are shown in Fig. 10 below.

6.1 Peak current mode control

Peak current mode control is the most simple and straight forward approach. It directly controls the peak of the inductor current to follow the envelope of the sinusoidal input voltage. Basically it works in the same manner as in those current-mode controlled regulator. However, in this case, instead compared with the dc level voltage error signal, the peak of the input current is compared with the sinusoidal reference current in the PWM comparator. The reference current follow the input voltage envelope. Its amplitude is controlled by the voltage error signal and the line voltage level to achieve line and load regulation of the output voltage. The implementation of peak current mode is simple and the control is more efficient. However, compensation ramp is required to apply to the reference current envelope for stable operation. Peak current mode control exhibits poor noise immunity and large peak to average current error. The inductor current of peak current mode control is shown in Fig. 11(a). Some available controller ICs for peak current mode control are ML4821 from Fairchild and TK84812 from Toko.

6.2 Average current mode control

Average current mode control introduced by Dixon, 1990 [10] controls the average input current (averaged over a few switching cycles) to follow the envelope of the sinusoidal input voltage. The average input current is compared with a reference current in a large bandwidth current error amplifier. The error signal is then fed into the PWM modulator, where it is compared with a fixed-frequency sawtooth generated from the clock. The reference current is programmed to have the same envelope or shape of the input sinusoidal voltage, while its amplitude is determined by the output voltage error and the input line level to achieve output regulation. Average current control can track the current program more accurately than peak current mode control. It also has a better noise immunity with the use of the sawtooth at the PWM modulator. However, the current loop is difficult to stabilize and require tuning for the compensation network. The loop gain is also limited. If the gain is too high, it will lead to oscillation. If the gain is too low, it can't track the reference current very well and results in high distortion. The inductor current of average current mode control is shown in Fig. 11(b). Some available controller ICs for average current mode control are Unitrode's UC3854 and Fairchild's ML4821.

6.3 Hysteretic current control

Hysteretic control involves the use of two reference currents, the upper reference and the lower reference current. The switch is turned off when the inductor current reaches the upper current reference and turned on when the current falls down to reach the lower reference current. The difference between the two reference (hysteresis) can be constant (fixed hysteretic control) or varies with the line voltage sinusoidal envelope. (variable hysteretic control). The inductor current of variable hysteretic current control is shown in Fig. 11(c). Transition mode control or borderline control is the modified version of hysteretic control, in which the boost PFC corrector is operating at the boundary mode (between DCM and CCM). The switch is turned off when the inductor current reach the reference current and is turned on again when the inductor current drops to zero. The biggest disadvantage of hysteretic control or borderline control is the variable switching frequency and they are mainly used in low power application. The inductor current of borderline control is shown in Fig. 11(d). Some available controller IC for transition mode or borderline current mode control are ST's L6561 and Unitrode's UC1852.

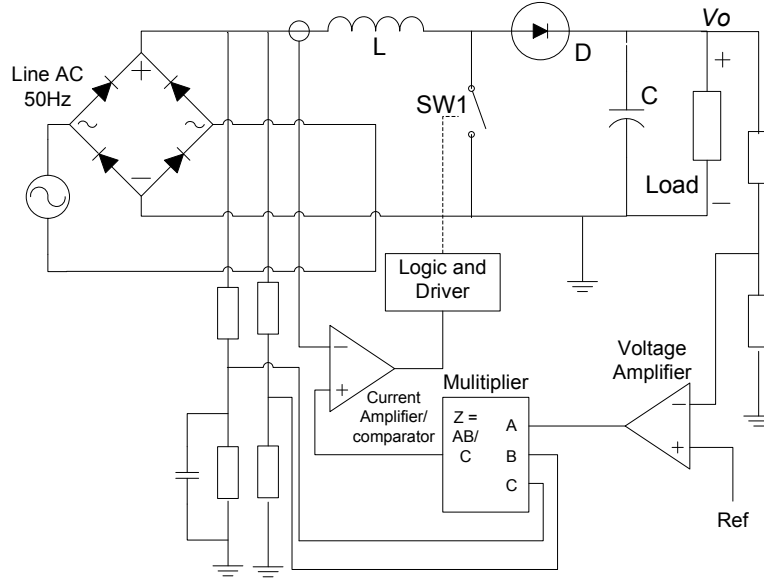


Figure 10: General scheme of active current control in boost corrector

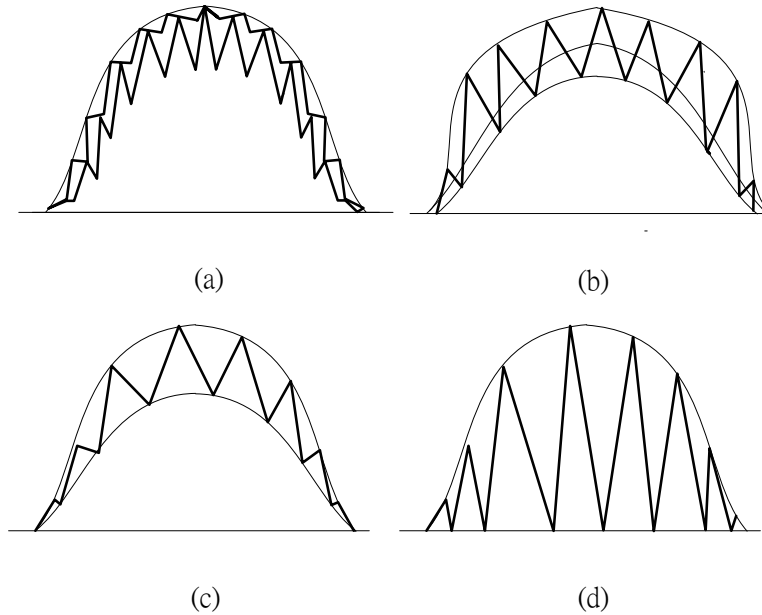


Figure 11: The inductor current waveform using various control methods

7 Stability Analysis and Bifurcation Behavior of Boost PFC

A single stage PFC is a two-loop control system: One of the loop is a slow outer voltage loop to regulate the output voltage, another is a fast inner current loop to shape the input current into line voltage envelope. Instability of the current loop results in the so called fast-scale bifurcation and shows the phenomenon of

period doubling among switching cycles. (several hundreds KHz) While instability of the voltage loop results in slow-scale bifurcation, which shows the phenomenon of period doubling among line cycles (50/60Hz).

Instability or bifurcation behaviors have been reported in boost PFC and quite a number of research and publications have been focusing on the stability analysis of the boost PFC. R. Ridley [11] provided a small signal model of boost PFC. Mazumder [12] developed a state-space model for boost PFC to analyze the converter stability in saturated and unsaturated regions using Lyapunov method and bifurcation analysis. Dranga and Tse [13] also demonstrated the fast-scale current loop bifurcation by simulation in boost PFC with peak current mode control. According to their result, duty cycle and the power converter's steady state gain (ratio of output voltage) and circuit parameter like inductor and the load resistance, etc affects stability. The stable/unstable regions have been identified, as well as the relationship of the critical phase angle and the dc converter gain.

For slow-scale bifurcation, Wong, Tse and Orabi [14] developed an average boost PFC model by double averaging and derived the slow-scale instability boundaries with different circuit parameters. Experiment was conducted and succeeded in verifying some of the stability boundaries derived. Based on their results, the PFC's stability becomes worse with higher output voltage to input voltage ratio, higher voltage loop dc gain, smaller voltage loop time constant and/or smaller output capacitor value.

8 Simulation of Boost PFC Pre-regulator

A Simulink model of an ideal boost PFC under average current model control was used by Dranga, 2002 [3] to demonstrate the PFC slow-scale bifurcation behavior as shown in fig 12. The stability boundaries of the single-stage pre-regulator and its cascaded system with a non-isolated buck converter are also identified and compared with different circuit parameters. The model of the single-stage boost PFC is shown in Fig 13 and some initial results are shown in Fig 14.

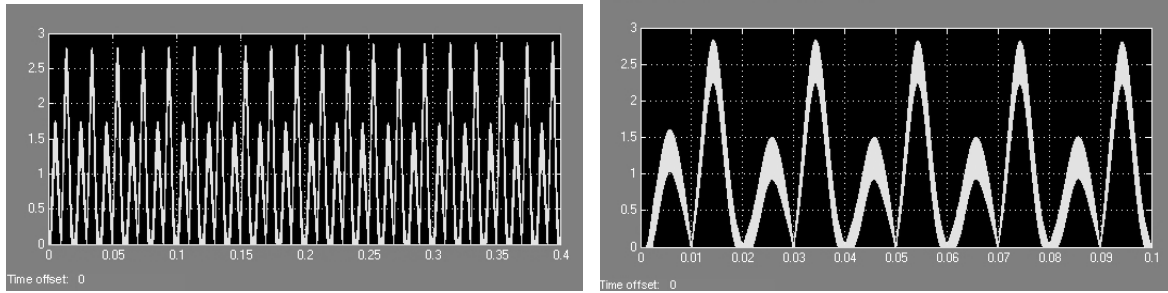


Figure 12: Slow-scale bifurcation or period doubling demonstrated by the simulation model [left] and the enlarged waveform [right]

One of the curves is repeated with the parameters shown in Table 1. The resulting plot shows some deviation from the initial results, especially in the high power region where almost all bifurcation seem to disappear. Further work need be done to investigate whether such deviation is due to some deficiency in the simulation model or some complex circuit behavior during high power stage. The resulting plots are shown in Fig 15.

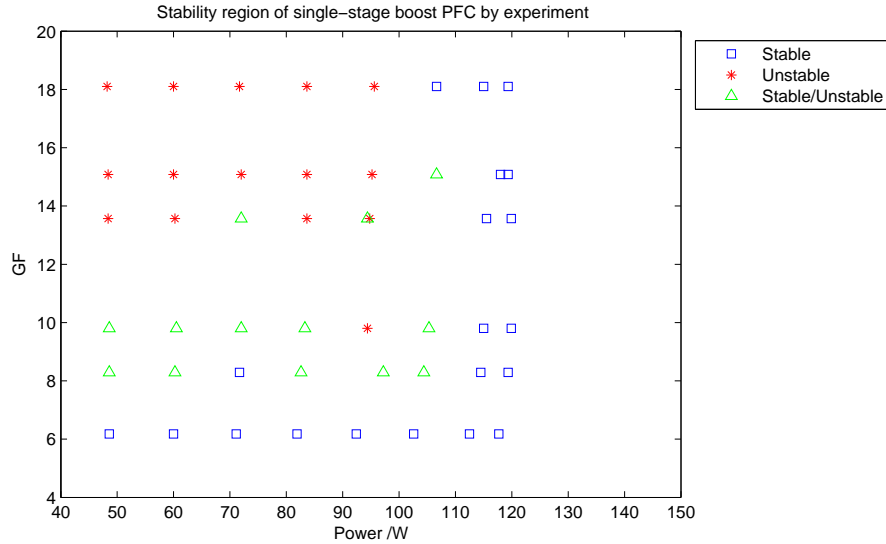


Figure 17: Stability region of single-stage boost PFC Pre-regulator by experiment

10 Conclusion

In this report, we have reviewed some fundamental concepts of PFC. Firstly, the importance of power factor correction in the society and the industry has been mentioned and the definition of power factor is presented. Then we have introduced some basic PFC converter topologies such as buck, boost and buck boost, with their advantages and disadvantages compared, as well as a few innovative topologies from the variation of the basic topologies. Besides, common control schemes for input current shaping has been reviewed. In later sessions, we have discussed the stability analysis and bifurcation behavior of a boost PFC. A Simulink model has been presented and used to identify the stability boundary of a boost PFC with average current mode control. The simulation is repeated and the resulting plot matches with the initial findings by Dranga [3] at the low power region; while large deviations found at the high power region. A single-stage boost PFC circuit is implemented with UC3854 controller IC for experimental verification. The experimental result has been presented and it matches with the simulation result.

Further work need to be done to verify the stability boundaries of a single-stage boost PFC and its cascaded system with a forward converter with transformer isolation. For the single-stage boost PFC pre-regulator, simulations need to be repeated to re-identify the slow-scale period doubling region. At the meantime, a new single-stage boost PFC pre-regulator needs to be built in order to verify the simulation result in high power region. The current challenges are the co-relation of transfer function's dc gain in the simulation model with the dc gain of the error amplifier in the real circuit, as well as how to change the output/input voltage ratio in the real circuit while keeping the dc gain constant. For the cascaded system, similarly, simulation can be repeated with the original model first to verify the initial results. Then the model can be adjusted (by adding transformer turn ratio) and compare it with the non-isolated version. Meanwhile a transformer-isolated forward converter need to be built to verify the simulation result. With the addition of the transformer, duty cycle can be adjusted by changing the transformer's turn ratio, while keeping the output voltage constant. Therefore, the effect of duty cycle on slow-scale bifurcation can be investigated more accurately.

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