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LETTER TO THE EDITOR

IMPLEMENTING EXTRA ELEMENT THEOREM USING NULLOR APPROACH

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SUMMARY

This letter presents a method of implementing the extra element theorem (EET) on the computer by using the nullor method. The EET involves the calculation of two driving-point impedances (dpi's), namely the conventional dpi, Z_d, and the null dpi, Z_n. The proposed method is used mainly for calculating Z_n. The method is simplified by representing any given circuit using exclusively RC-nullor and R-nullor equivalent circuits, thereby permitting the use of a single (parallel) version of the EET. The proposed method is applied to the linearized boost converter model to derive the fragmented version of the duty-ratio-to-output transfer function. Copyright © 1999 John Wiley & Sons, Ltd.

1. INTRODUCTION

The extra element theorem (EET)[1,2] states that given a transfer function of a linear network N, the likewise defined transfer function of a network N', which is formed by adding an extra element Z to N, can be expressed as the product of the transfer function of N and a *correction factor* which involves the extra element and two driving-point impedances (dpi's) seen at the node pair where the extra element is inserted.

In practice, the EET proves advantageous if the calculation of the two dpi's are easier than the direct calculation of the desired transfer function. While there is no guarantee, this is usually the case. In addition, the EET is useful in illuminating the relative contribution of the extra element to the desired transfer function or the network response.

The EET requires the calculation of two driving-point impedances (dpi's) seen at the port where an extra element is to be inserted, viz., the conventional Thévenin impedance, Z_d, and the null dpi, Z_n. The calculation of Z_d is relatively easier to do on the computer than by hand. The null dpi is the impedance seen at the extra element port under the null output condition obtained by adjustment of original input and the other input at the extra element port. The method of obtaining Z_n, as explained in Reference 1, is easy by hand calculation but the same method cannot be implemented on the computer, because it requires thorough logical inference and deduction based on circuit theory. This is the principal motivation of this letter to derive a method for implementing the EET on the computer. In particular, the method described in this letter uses the simple concept of nullors.

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2. THE NULLOR APPROACH TO IMPLEMENTING EET

2.1. Versions of EET

There are two versions of the EET for parallel and series extra elements.[1] In the first version, we consider a network N, to which an extra element is to be inserted in parallel. Suppose A is a transfer function of the network. The EET gives the formula for A, after the extra element is added in parallel, as

$$A|_Z = A|_{Z=\infty}\left(\frac{1 + Z_n/Z}{1 + Z_d/Z}\right) \tag{1}$$

where Z is the impedance of the extra element to be added in parallel. In the second version, we consider an extra element is to be inserted in series to a branch in the network. In this case, the EET gives the formula for A, after the extra element is added in series, as

$$A|_Z = A|_{Z=0}\left(\frac{1 + Z/Z_n}{1 + Z/Z_d}\right) \tag{2}$$

where Z is the impedance of the extra element to be added in series.

2.2. Calculation of Z_d

Z_d can be easily found by the conventional method of calculating the Thévenin impedance. This requires the shorting of all independent voltage sources and opening of all independent current sources. Then, a current or voltage source is inserted across the the extra element port and the admittance matrix equation is solved for Z_d.

2.3. Calculation of Z_n

The nullor method is proposed here for the calculation of Z_n. This method is usually used in the analysis and design of RC-active circuits.[3,4] The nullor, as shown in Figure 1, is a two-port combination of a norator and a nullator. A nullator has both its terminal voltage and current equal to zero, whereas a norator has an arbitrary branch-voltage–current relationship (BVCR).

The arbitrary BVCR property of the norator is exploited here to calculate the null dpi. In other words, the norator has the property to assume to itself any value of voltage and current depending on the conditions of the embedded network. Hence, the norator can be regarded as an arbitrary voltage source.

The nullator is inserted across the node pair whose output is to be nulled, while the norator is inserted across the node pair where the extra element, Z, is inserted. Hence, the driving point impedance seen by the norator is the null dpi, Z_n. In the proposed algorithm we consider the norator current as an unknown. This constrains us to use the modified nodal admittance (MNA) method with the norator current as an unknown which is to be found. Then, the matrix equation is solved for the norator voltage and current to get the value of Z_n.

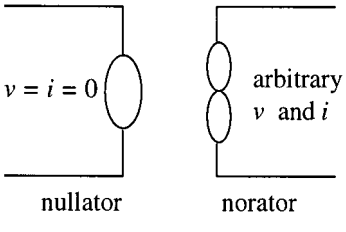

Figure 1. The nullor

In our nullor approach, as mentioned earlier, the null condition is imposed by an external element, namely the nullator. This differs from the method introduced by Middlebrook[1] where the two input sources, i.e., the original input and the test source across the extra element port, are adjusted in phase and/or magnitude to get the null condition. Here our attention is focused on developing a simple and efficient algorithm that can be implemented on the computer.

3. ALGORITHM FOR CALCULATION OF Z_n

In this section we outline an algorithm, to which we refer as modified nullor-nodal admittance (MNNA) matrix contraction, for calculating Z_n. Assuming that the given circuit is well posed and not disconnected,[5] the following steps are taken:

1. Construct the MNA matrix of the given circuit.
2. Insert a nullator across the node pair whose voltage or current is to be nulled.
3. Insert a norator across the node pair where the extra element is to be inserted.
4. Add the columns of the MNA matrix corresponding to the nullator node pair and delete the column corresponding to the nulled voltage of the nullator node pair.
5. Delete the entry of the nulled unknown variable corresponding to the deleted column of step 4 in the column matrix in the LHS.
6. Solve for the norator's node voltages and the current through the norator.
7. Divide the node voltage difference by the norator current to get the null dpi Z_n.

We can actually simplify the matrix further if one of the nodes of the output port is connected to the datum reference node (i.e. common datum reference node with the input port). This can be accomplished by deleting the corresponding column of the non-datum reference node voltage of the output port without adding any columns in the nodal matrix.

In the next section we will simplify the method by modelling the circuit appropriately so that only current sources, capacitors, resistors and nullors need to be dealt with.

4. RC-NULLOR CIRCUITS

The algorithm described in Section 3 can be simplified by modelling the given circuit using exclusively RC-nullor and R-nullor circuits[3]. The procedure of constructing the equivalent circuit is straightforward. Each device in the circuit will be replaced by an RC-nullor or an *R*-nullor equivalent circuit. The reason for doing this is to allow the use of a single version of (parallel) EET formula, since the only type of reactive elements in the equivalent model will be capacitance. Then, using the EET for parallel insertion, the desired transfer function is

$$A|_{Z=1/sC} = A|_{Z=\infty}\left(\frac{1+sCZ_n}{1+sCZ_d}\right) \tag{3}$$

The use of only the parallel version of EET obviously reduces the number of subroutines involved in the calculation of dpi's, especially when there is more than one element to be inserted for the same transfer function. This feature will be exemplified in the next section.

5. ILLUSTRATIVE EXAMPLE

A linearized boost switching converter model with perturbation in the duty ratio is considered as an example.[6] The boost converter is a step-up converter containing a pair of switches which are turned on and off in an orderly and complementary manner to produce a sequence of circuit topologies. The usual analysis

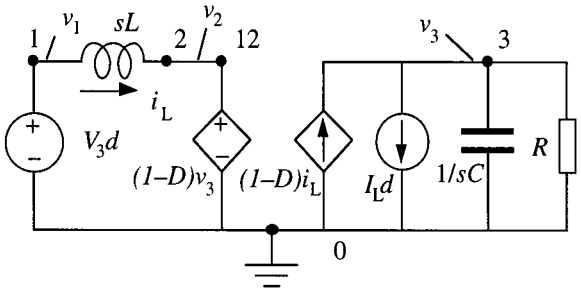

Figure 2. Linearized boost converter with perturbation in duty ratio d. (Upper-case letters denote steady-state values and lower-case letters denote small-signal variables. Additional node 12 is created for current sensing)

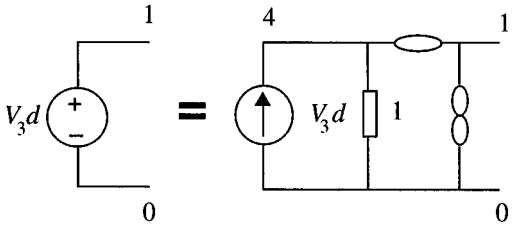

Figure 3. R-nullor current source equivalent circuit for the voltage source. (Additional node 4 introduced)

technique for switching converters involves 'averaging' and 'linearization', which generate a small-signal model for subsequent application of linear analysis techniques. A typical model of the boost converter is shown in Figure 2. This model contains reactive elements and controlled sources, and is therefore a suitable yet simple example to illustrate our proposed method. In this circuit, the duty ratio, d, is the parameter used to control the output voltage, v_3. The model is also quite interesting as it predicts a non-minimum phase response in the case of the boost converter for any perturbation in the duty ratio. Our aim is to get the transfer function v_3/d. The algorithm described in Section 3 is applied as follows:

1. The nodes of the boost converter circuit are numbered from 0 to 3, as shown in Figure 2. Node 12 is included here to allow the inductor current to be sensed by the current-controlled-current-source. The first step is to replace this circuit by an equivalent circuit containing only current sources, nullors, resistors and capacitors. First, the voltage source is replaced by an equivalent circuit consisting of a current source, a nullor and a resistor, as shown in Figure 3. Second, the inductor is replaced by an RC-nullor equivalent circuit (i.e. capacitor-terminated gyrator), as shown in Figure 4. Third, the controlled sources are replaced by appropriate R-nullor equivalent circuits, as shown in Figures 5 and 6.
2. The capacitor in the inductor equivalent circuit (Figure 4) and the load capacitor between nodes 3 and 0 (Figure 2) are designated as extra elements. By performing the matrix contraction due to nullors[3] and removing all the unwanted norator currents from the admittance matrix equation, we get the reference admittance matrix equation, in the absence of the extra elements, as

$$\begin{bmatrix} 0 & 0 & 1/R & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 \\ 0 & 1/D_2 & -1 & 0 & 0 \\ 0 & -1 & 0 & 1 & 1/D_2 \end{bmatrix} \begin{bmatrix} v_{1,4} \\ v_{2,5,7,12} \\ v_{3,8} \\ v_6 \\ v_{9,10} \end{bmatrix} = \begin{bmatrix} -I_Ld \\ V_3d \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{4}$$

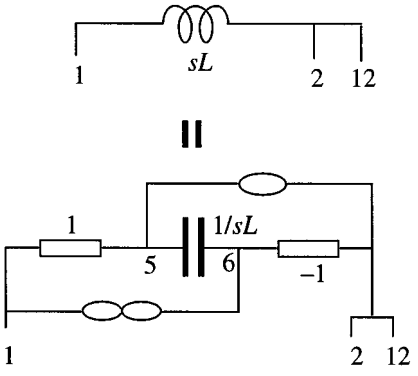

Figure 4. RC-nullor equivalent circuit for the inductor. (Node 12 to be connected to the R-nullor equivalent circuit of the current-controlled-current-source shown in Figure 5)

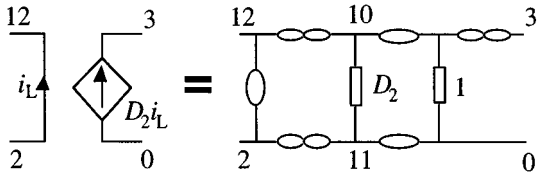

Figure 5. R-nullor equivalent circuit for the current-controlled-current-source. (Nodes 2 and 12 are the same points in the original circuit, and are used here for current sensing)

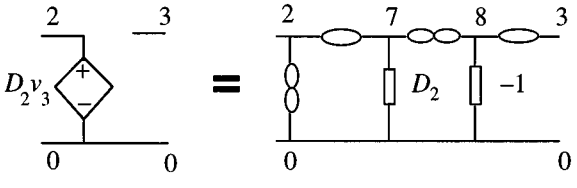

Figure 6. R-nullor equivalent circuit for the voltage-controlled-voltage-source

Thus, the transfer function in the absence of reactive elements can be obtained from the matrix equation as

$$\left.\frac{v_3}{d}\right|_{\text{without } L \text{ and } C} = \frac{V_3}{D_2} = \frac{V_{\text{in}}}{D_2^2} \tag{5}$$

where $D_2 = 1 - D$, $V_3 = V_{\text{in}}/D_2$, and V_{in} is the DC input voltage (not shown in the diagrams).

3. Now let us consider the inductor (capacitor in the equivalent representation shown in Figure 4) as an extra element. Calculation of Z_d requires deleting the first two rows of the RHS of (4) and placing a single current source entry, i_{t1}, on the third row, corresponding to nodes 5 and 6 where the extra element is to be

inserted. Then, the resulting matrix equation becomes

$$\begin{bmatrix} 0 & 0 & 1/R & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 \\ 0 & 1/D_2 & -1 & 0 & 0 \\ 0 & -1 & 0 & 1 & 1/D_2 \end{bmatrix} \begin{bmatrix} v_{1,4} \\ v_{2,5,7,12} \\ v_{3,8} \\ v_6 \\ v_{9,10} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ i_{t1} \\ 0 \\ 0 \end{bmatrix} \tag{6}$$

After solving for v_5, v_6 and i_{t1}, we get the required Thévenin dpi as

$$Z_{\mathrm{d}} = \frac{v_6 - v_5}{i_{t1}} = \frac{1}{D_2^2 R} \tag{7}$$

4. Next we need to find the null dpi Z_{n}. A norator is placed across nodes 5 and 6, and a nullator is placed across output port nodes 3 and 0. The matrix equation becomes

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & -1 \\ 0 & 1/D_2 & 0 & 0 & 0 \\ 0 & -1 & 1 & 1/D_2 & 1 \end{bmatrix} \begin{bmatrix} v_{1,4} \\ v_{2,5,7,12} \\ v_6 \\ v_{9,10} \\ i_{n1} \end{bmatrix} = \begin{bmatrix} -I_{\mathrm{L}} d \\ V_3 d \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{8}$$

where $i_{\mathrm{n}1}$ is the current in the norator between nodes 5 and 6. After solving for $i_{\mathrm{n}1}$, v_5 and v_6, we get the required null dpi as

$$Z_{\mathrm{n}} = \frac{v_6 - v_5}{i_{\mathrm{n}1}} = \frac{-I_L}{D_2 V_3} = \frac{-1}{D_2^2 R} \tag{9}$$

since $I_{\mathrm{L}} = V_3/D_2 R$. Putting (5), (7) and (9) in (3), we get

$$A\,|_{\text{with } L} = \frac{V_{\mathrm{in}}}{D_2^2}\left[\frac{1 - sL/D_2^2 R}{1 + sL/D_2^2 R}\right] \tag{10}$$

At this stage we note that the EET has already revealed the non-minimum phase characteristics of the duty-ratio-to-output transfer function of the boost converter, as illustrated in (10).

5. Steps 3 and 4 are repeated to insert the load capacitor between nodes 3 and 0. In particular, we need to construct the admittance matrix for the circuit with the inductor present. In calculating Z_{d}, the admittance matrix equation is

$$\begin{bmatrix} 0 & 0 & 1/R & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 1+sL & 0 & -sL & 0 \\ 0 & 1/D_2 & -1 & 0 & 0 \\ 0 & -1 & 0 & 1 & -1/D_2 \end{bmatrix} \begin{bmatrix} v_{1,4} \\ v_{2,5,7,12} \\ v_{3,8} \\ v_6 \\ v_{9,10} \end{bmatrix} = \begin{bmatrix} i_{t2} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{11}$$

where i_{t2} is the test current source inserted between nodes 3 and 0. After solving for v_3 and i_{t2}, we get the required Thévenin dpi as

$$Z_{\mathrm{d}} = \frac{v_3}{i_{t2}} = \frac{sLR}{sL + D_2^2 R} \tag{12}$$

Likewise, in calculating Z_n, we need to construct the admittance matrix equation as in step 4, and solve for v_3 and the norator current, i_{n2}, inserted between nodes 3 and 0. The required null dpi is

$$Z_n = 0 \tag{13}$$

since $v_3 = 0$ and $i_{n2} \neq 0$.

Finally, putting (10), (12) and (13) in (3), we obtain the final transfer function as

$$A\,|_{\text{with } L \text{ and } C} = \frac{v_3}{d}\bigg|_{\text{with } L \text{ and } C} = \frac{V_{in}}{D_2^2}\left[\frac{1 - sL/D_2^2R}{1 + sL/D_2^2R}\right]\left[\frac{1}{1 + s^2LRC/(sL + D_2^2R)}\right] \tag{14}$$

Further simplifying (if necessary), we get

$$A\,|_{\text{with } L \text{ and } C} = \frac{V_{in}}{D_2^2}\left[\frac{1 - sL/D_2^2R}{1 + sL/D_2^2R + s^2LC/D_2^2}\right] \tag{15}$$

which is the transfer function we wish to find.

6. CONCLUSION

A computer-oriented implementation of the extra element theorem by using the nullor method is discussed. The method is simplified by using exclusively RC-nullor and R-nullor circuits, thereby facilitating the use of a single (parallel) version of EET. This further simplifies the subroutine. A non-minimum phase boost converter is used to illustrate the derivation of the fragmented version of the duty-ratio-to-output transfer function, i.e. the DC transfer function and the pole/zero (correction factor) part. Without analysing the entire circuit, the EET highlights the behaviour of the non-minimum phase system by exposing the RHP zero. In complex circuits, the EET plays a major role in exposing the important properties owing to a particular reactive element or any other element that has been designated as an 'extra' element. This enables the analogue circuit designers to carry out their jobs expeditiously.

ACKNOWLEDGEMENT

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