An Analog Implementation to Improve Load Transient Response of PFC Pre-regulators

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Abstract—This paper presents an analog implementation to improve the load transient response of PFC pre-regulators. By means of a notch filter inserted between the output-voltage sensing network of the pre-regulator and the voltage control loop of the pre-regulator control circuitry, the bandwidth of the voltage control loop is greatly expanded without introducing extra input current harmonics into the pre-regulators. This approach uses operational amplifiers with R-C networks to realize the notch filter, therefore it can be implemented into the existing pre-regulators with minor modification. The notch filter can be applied in both continuous-conduction-mode (CCM) pre-regulators and discontinuous-conduction-mode (DCM) pre-regulators. Furthermore the size of the output capacitor of the pre-regulators can be reduced due to the expanded bandwidth of the voltage control loop. The improved load transient response of the analog notch filter is observed experimentally. A laboratory prototype of a 100W DCM flyback pre-regulator has been built to illustrate the benefits of this cost-effective solution.

I. INTRODUCTION

A common method to achieve power factor correction (PFC) is to use a continuous-conduction-mode (CCM) boost converter with average current-mode (ACM) control [1] for medium to high power applications. Alternatively, a discontinuous-conduction-mode (DCM) flyback converter with voltage mode control [2] is also commonly used for low power applications. In any PFC pre-regulator, the output voltage inevitably contains the second-harmonic (100 Hz or 120 Hz) ripple voltage. This can be easily explained by Tellegen's theorem [3], which concludes that the sum of powers of all branches of the pre-regulator is zero. A power flow diagram of the PFC pre-regulator is depicted in Fig. 1. The power balance of the pre-regulator can be expressed as

$$v_{in} i_{in} \sin^2 \omega t = \frac{P_{in}(1 - \cos 2\omega t)}{2} = \frac{V_{out}^2}{R_{Load}}, \quad (1)$$

where P_{in} , V_{out} , and R_{Load} are the peak input power, the output voltage, and the load, respectively, of the pre-regulator, and ω is the angular frequency of the input voltage. Since the output power is composed of a dc component and an ac component at twice of the ac mains frequency, the second-harmonic ripple voltage appears at the output capacitor. This ripple voltage cannot be compensated by the voltage control loop without causing the input current distortion. Therefore, the bandwidth of the pre-regulator voltage control loop is placed around one fifth [4] of the ac mains frequency, the main drawback is that the pre-regulator provides slow load

Fig. 1. Power-factor-corrected pre-regulator power flow diagram.

transient response, and the output capacitor will require to store substantial energy to support the transient load.

To respond quickly to load disturbances without distorting the input current during steady-state operation, several techniques have been proposed in the literature [5], [6]. Some proposed solutions aim to eliminate the ripple voltage from the output voltage feedback signal by a ripple compensation technique [7]–[9]. The bandwidth of the voltage control loop can be greatly expanded, however, the technique is accomplished by a complicated controller to synchronize the phase of the ripple voltage and to detect the ripple voltage level. Sliding mode control [10] and boundary control [11] were proposed which allow faster load transient response, but these methods require the pre-regulator to operate with variable switching frequency. The use of an extra voltage control loop for decreasing the output impedance of the pre-regulator was reported [12]. The method improves the load transient response without the need for a wide bandwidth voltage control loop, but the load transient response improvement is less effective as compared to the aforementioned methods.

The notch filter method has also been widely discussed in [13] and [14]. Unfortunately, the filters proposed in these works were implemented by a micro-controller [13] and a digital signal processor [14]. The major drawback is that the existing pre-regulator requires a complete redesign in their control circuitry to enjoy the advantages of the notch filter. Our objective in this paper is to apply a notch filter constructed by an analog circuit and consequently the existing controller can be slightly modified to improve the load transient response of the PFC pre-regulator.

II. NOTCH FILTER

Fig. 2 depicts the simplified connection diagram of the pre-regulator with an analog notch filter. The notch frequency of the filter is fixed as twice the ac mains frequency in

Fig. 2. Simplified connection diagram of the pre-regulator with the notch filter.

order to attenuate the second-harmonic ripple voltage of the voltage error amplifier input. As a result, the bandwidth of the voltage control loop can be expanded to improve the load transient response. On the other hand, the filter reveals that the expanded voltage control loop cannot improve the load transient response at twice the input voltage frequency.

The general transfer function of the notch filter [15] is represented by

$$H_N(s) = \frac{s^2 + \omega_o^2}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2}, \quad (2)$$

where ω_o is the angular notch frequency and Q controls the filter bandwidth of the notch frequency. An analog notch filter based upon a modified twin tee network is depicted in Fig. 3. The operational amplifiers, OP1 and OP2, are connected as voltage followers to reduce the loading effect. From Fig. 3, assuming that

$$\begin{aligned} R &= R_A = R_B = 2R_C, \\ C &= \frac{C_A}{2} = C_B = C_C, \\ \beta &= \frac{R_E}{R_D + R_E}, \end{aligned}$$

the transfer function of the twin tee network can be derived as

$$\frac{V_o}{V_{out}} = \frac{s^2 + (\frac{1}{RC})^2}{s^2 + s\frac{1}{RC}(1 - \beta)4 + (\frac{1}{RC})^2}, \quad (3)$$

where V_{out} is the output voltage of the pre-regulator and V_o is the filtered voltage to the voltage error amplifier. We compare (3) with the general notch filter transfer function (2). Equating like terms give

$$\omega_o = \frac{1}{RC} \quad (4)$$

and

$$Q = \frac{R_D + R_E}{4R_D}. \quad (5)$$

The notch frequency can be evaluated as

$$f_o = \frac{1}{2\pi RC} \quad (6)$$

and then the filter bandwidth is expressed as

$$BW = \frac{f_o}{Q}. \quad (7)$$

Fig. 3. Adjustable Q notch filter implemented by analog circuit.

III. PRE-REGULATOR MODELING AND ANALYSIS

A. CCM Boost Pre-regulator Under ACM Control

ACM PFC controller consists of two interconnected control loops [1], which are the inner current control loop and the outer voltage control loop. In this discussion, our consideration aims of the voltage control loop and assumes that the input current loop provides the “ideally shaped” sinusoidal current.

Based on our assumption, Fig. 4 depicts a large-signal model [16] for the CCM boost pre-regulator. The input port characteristic of the pre-regulator is simulated by the loss-free resistor, R_{ec} , to maintain the sinusoidal current. This resistor is made by a wide-bandwidth current control loop. The value of R_{ec} can be found by

$$\frac{v_{in}|\sin \omega t|}{i_{in}|\sin \omega t|} = R_{ec}c(t) \quad (8)$$

where $v_{in}|\sin \omega t|$ and $i_{in}|\sin \omega t|$ are the rectified input voltage and input current, respectively, and $c(t)$ is a signal to control the resistance R_{ec} depending on the voltage error amplifier output and the rms value of the input voltage. The function of the voltage control loop is to keep the output voltage, V_{ccm} , regulated by changing R_{ec} . The output power source, P_{ccm} , can be written as

$$P_{ccm} = \frac{(v_{in}|\sin \omega t|)^2}{R_{ec}c(t)}. \quad (9)$$

Thus, the output current, I_{ccm} , is given by

$$I_{ccm} = \frac{(v_{in}|\sin \omega t|)^2}{V_{ccm}R_{ec}c(t)}, \quad (10)$$

Fig. 4. Large signal model with the loss-free resistor representing the CCM boost pre-regulator under ACM control.

Fig. 5. Large signal model of DCM flyback pre-regulator under voltage-mode control.

where V_{ccm} is the dc value of the output voltage. Also, $c(t)$ of the CCM boost pre-regulator can be expressed as

$$c(t) = \frac{G_{\text{ccm}} v_{\text{erc}}}{v_{\text{in,rms}}^2}, \quad (11)$$

where v_{erc} , $v_{\text{in,rms}}$, and G_{ccm} are the error voltage, the rms value of the input voltage, and the gain of voltage error amplifier, respectively.

B. DCM Flyback Pre-regulator Under Voltage-Mode Control

A large-signal model that represents a DCM flyback pre-regulator under voltage-mode control by using a loss-free resistor is shown in Fig. 5 [2]. The input port of the DCM flyback pre-regulator behaves inherently as a pure resistor. The equivalent resistance of the input port is given by

$$R_{\text{ed}} = \frac{2Lf_s}{D^2}, \quad (12)$$

where L , f_s , and D are the inductance of the input inductor, the switching frequency, and the duty cycle, respectively, of the pre-regulator. Therefore, the resistance can be controlled by varying of the duty cycle. The output power source can be evaluated by

$$P_{\text{dcm}} = \frac{(v_{\text{in}} |\sin \omega t|)^2}{R_{\text{ed}}}, \quad (13)$$

and the output current is given by

$$I_{\text{dcm}} = \frac{(v_{\text{in}} |\sin \omega t|)^2}{2L f_s V_{\text{dcm}}} D^2, \quad (14)$$

where $v_{\text{in}}|\sin \omega t|$ and V_{dcm} are the rectified input voltage and the dc value of the output voltage, respectively. The duty cycle of the DCM flyback pre-regulator can be expressed as

$$D = v_{\text{erd}} \frac{G_{\text{dcm}}}{V_{\text{ramp}}}, \quad (15)$$

where v_{erd} , G_{dcm} , and V_{ramp} are the error voltage, the gain of the voltage error amplifier, and the peak-to-peak voltage of the ramp signal, respectively, of the DCM flyback pre-regulator.

Fig. 6. Simple compensation network is employed for the expanded voltage control loop.

TABLE I
SPECIFICATION OF DCM FLYBACK PRE-REGULATOR.

Description	Value
Input voltage	110 V_{rms}
The ac mains frequency	60 Hz
Maximum output power	100 W
Output voltage	48 V
Switching frequency	100 kHz

C. Redesign of Voltage Control Loop of PFC Controller

A small signal model applicable for frequencies below the line frequency and useful for designing the standard voltage control loop can be found in [18], [19]. However this model is invalid for frequencies above the ac mains frequency. The bandwidth of the expanded voltage control loop is higher than the ac mains frequency. So the traditional compensator design technique based on the small signal model is inappropriate to the expanded voltage control loop. Our approach of designing the expanded voltage control loop is based on computer simulations and experimental measurements. A simple PI control is employed for the expanded voltage control loop, as shown in Fig. 6. The transfer function of the expanded voltage control loop is given by

$$\frac{v_{\text{ero}}}{v_{\text{erd}}} = \frac{sR_{\text{c}2}C_{\text{c}1} + 1}{s^2R_{\text{c}1}R_{\text{c}2}C_{\text{c}1}C_{\text{c}2} + sR_{\text{c}1}(C_{\text{c}1} + C_{\text{c}2})}. \quad (16)$$

The improved load transient response is proven by experimental verification as documented in Section IV.

IV. EXPERIMENTAL RESULTS

In this section, a DCM flyback pre-regulator is used as an example to demonstrate the advantage of the expanded voltage control loop with the analog notch filter. The specification of the pre-regulator is shown in Table I. The simplified schematic of the experimental prototype is shown in Fig. 7. Two voltage model control circuitries are built. One circuitry uses a quad-operational-amplifier IC, LM324, to construct the voltage error amplifier with the notch filter. The notch frequency is designed at 120 Hz and the Q factor of the filter is 10. Fig. 8 shows the magnitude and the phase characteristics of the expanded voltage control loop with the notch filter. In this control loop, the zero is placed around 54.4 Hz and the pole is placed around 2.12 kHz. Another circuitry uses a dual-operational-amplifier IC, LM358, to construct the voltage error amplifier without the notch filter. As mention in Section I, the wide bandwidth of the voltage control loop causes the input current

Fig. 7. Simplified schematic of the experimental prototype.

Fig. 8. Magnitude and phase characteristics of the expanded voltage control loop with the notch filter.

harmonic distortion, for providing a comparison, we have been measured the power factor and tuned the compensation networks of these two voltage error amplifiers to provide similar power factor at different power levels at steady state output power condition, as shown in Table II. Therefore, there is no significant difference of the performance of the two control circuitries from the ac mains viewpoint.

Fig. 9 exhibits a comparison of the output voltage regulation of the DCM flyback pre-regulator between using the expanded bandwidth voltage control loop with the notch filter and using

Fig. 9. Measured load regulation comparison between the expanded bandwidth voltage control loop with the notch filter and the standard voltage control loop without the notch filter.

the standard voltage control loop without the notch filter. The load regulation of the pre-regulator with the expanded bandwidth voltage control loop is 0.38%, but the load regulation of the pre-regulator with the standard voltage control loop is 0.81%.

Figs. 10 (a) and (b) show the measured waveforms for a load stepping from 50 W to 100 W of the DCM pre-regulator with the expanded bandwidth voltage control loop with the notch filter and the standard voltage control loop without the notch filter, respectively. In Fig. 10 (a), the overshoot output

Fig. 10. Transient response for the change of load from 100 W to 50 W: (a) the expanded bandwidth voltage control loop with the notch filter and (b) the standard voltage control loop without the notch filter. Upper trace is the output voltage ripple, middle trace is the load current, and lower trace is the input current. The output capacitance is 4500 μ F. Time scale is 50 ms/div.

Fig. 11. Transient response for the change of load from 50 W to 100 W: (a) the expanded bandwidth voltage control loop with the notch filter and (b) the standard voltage control loop without the notch filter. Upper trace is the output voltage ripple, middle trace is the load current, and lower trace is the input current. The output capacitor value is 4500 μ F. Time scale is 50 ms/div.

voltage is $5.5 V_{pp}$ and the settling time is around 100 ms. Figs. 11 (a) and (b) show the measured waveforms at the load change from 100 W to 50 W of the DCM pre-regulator with the expanded bandwidth voltage control loop and the standard voltage loop, respectively. In Fig. 11 (a), the dropped output voltage is $5 V_{pp}$ and the settling time is around 130 ms. The

load transient response of the control loop with the notch filter is much better than the standard control loop.

Fig. 12 shows the comparative experimental response of the output voltage to a load step from 50 W to 100 W with both the expanded bandwidth voltage control loop with the notch filter (Figs. 12 (a) to (d)) and the standard voltage control loop (Figs. 12 (e) to (h)) at different output capacitor values. The value of the output capacitor has negligible influence on the transient voltage drop of the DCM pre-regulator with the expanded voltage control loop. However, with small capacitors, the input current harmonic is deteriorated in the case of the DCM pre-regulator with the expanded bandwidth voltage control loop. A tabulation of the data showing the properties of the DCM pre-regulator with the expanded voltage control loop and with the standard voltage control loop at different values of the output capacitor are given in Table III and Table IV, respectively. These tables show that the load transient response of the expanded voltage control loop is relatively faster than the standard one.

As mentioned in Section III-C, the traditional small signal model cannot elaborate on the accurate behavior of the DCM pre-regulator after the ac mains frequency. Hence, the experi-

TABLE II
MEASURED POWER FACTOR (P.F.) AND INPUT CURRENT TOTAL
HARMONIC DISTORTION (THD%)

P_{out} (W)	P.F. with N.F. (THD%)	P.F. without N.F. (THD%)
10	0.824 (10.50%)	0.814 (10.61%)
20	0.938 (6.57%)	0.931 (6.33%)
30	0.968 (5.14%)	0.963 (4.58%)
40	0.981 (3.97%)	0.977 (4.22%)
50	0.987 (3.47%)	0.984 (3.96%)
60	0.989 (3.17%)	0.988 (4.07%)
70	0.991 (3.52%)	0.990 (4.27%)
80	0.992 (4.48%)	0.991 (4.28%)
90	0.992 (4.82%)	0.992 (4.72%)
100	0.993 (4.77%)	0.993 (4.57%)

(a) Time scale is 50 ms/div.

(e) Time scale is 200 ms/div.

(b) Time scale is 50 ms/div.

(f) Time scale is 200 ms/div.

(c) Time scale is 50 ms/div.

(g) Time scale is 200 ms/div.

(d) Time scale is 50 ms/div.

(h) Time scale is 200 ms/div.

Fig. 12. Experimental waveforms of the DCM pre-regulator for step load change from 50 W to 100 W with different output capacitor values. (a)-(d) the expanded bandwidth voltage control loop with the notch filter and (e)-(h) the standard voltage control loop without the notch filter.

TABLE III

LOAD TRANSIENT PROPERTIES OF THE DCM PRE-REGULATOR WITH THE EXPANDED VOLTAGE CONTROL LOOP AT DIFFERENT VALUES OF OUTPUT CAPACITOR.

Output Capacitance (μF)	Load Change from 50 W to 100 W	Load Change from 100 W to 50 W	P.F. and THD% at 100 W Output Power
4500	$\Delta T_{\text{st}}=100 \text{ ms}$, $\Delta V_{\text{o pp}}=5.5 \text{ V}$	$\Delta T_{\text{st}}=130 \text{ ms}$, $\Delta V_{\text{o pp}}=5.0 \text{ V}$	0.993, 4.77%
3000	$\Delta T_{\text{st}}=80 \text{ ms}$, $\Delta V_{\text{o pp}}=6.0 \text{ V}$	$\Delta T_{\text{st}}=110 \text{ ms}$, $\Delta V_{\text{o pp}}=5.0 \text{ V}$	0.990, 6.99%
2400	$\Delta T_{\text{st}}=70 \text{ ms}$, $\Delta V_{\text{o pp}}=6.0 \text{ V}$	$\Delta T_{\text{st}}=90 \text{ ms}$, $\Delta V_{\text{o pp}}=6.0 \text{ V}$	0.989, 7.34%
2000	$\Delta T_{\text{st}}=65 \text{ ms}$, $\Delta V_{\text{o pp}}=7.0 \text{ V}$	$\Delta T_{\text{st}}=65 \text{ ms}$, $\Delta V_{\text{o pp}}=4.5 \text{ V}$	0.988, 7.77%
1640	$\Delta T_{\text{st}}=40 \text{ ms}$, $\Delta V_{\text{o pp}}=8.75 \text{ V}$	$\Delta T_{\text{st}}=50 \text{ ms}$, $\Delta V_{\text{o pp}}=7.5 \text{ V}$	0.988, 7.89%
1360	$\Delta T_{\text{st}}=40 \text{ ms}$, $\Delta V_{\text{o pp}}=8.75 \text{ V}$	$\Delta T_{\text{st}}=40 \text{ ms}$, $\Delta V_{\text{o pp}}=7.5 \text{ V}$	0.987, 8.31%
940	$\Delta T_{\text{st}}=25 \text{ ms}$, $\Delta V_{\text{o pp}}=12.5 \text{ V}$	$\Delta T_{\text{st}}=30 \text{ ms}$, $\Delta V_{\text{o pp}}=8.75 \text{ V}$	0.986, 8.71%
660	$\Delta T_{\text{st}}=25 \text{ ms}$, $\Delta V_{\text{o pp}}=15.75 \text{ V}$	$\Delta T_{\text{st}}=25 \text{ ms}$, $\Delta V_{\text{o pp}}=11.25 \text{ V}$	0.982, 10.23%
440	$\Delta T_{\text{st}}=20 \text{ ms}$, $\Delta V_{\text{o pp}}=17.5 \text{ V}$	$\Delta T_{\text{st}}=25 \text{ ms}$, $\Delta V_{\text{o pp}}=12.25 \text{ V}$	0.973, 13.75%

TABLE IV

LOAD TRANSIENT PROPERTIES OF THE DCM PRE-REGULATOR WITH THE STANDARD VOLTAGE CONTROL LOOP AT DIFFERENT VALUES OF OUTPUT CAPACITOR.

Output Capacitance (μF)	Load Change from 50 W to 100 W	Load Change from 100 W to 50 W	P.F. and THD% at 100 W Output Power
4500	$\Delta T_{\text{st}}=300 \text{ ms}$, $\Delta V_{\text{o pp}}=7.0 \text{ V}$	$\Delta T_{\text{st}}=4500 \text{ ms}$, $\Delta V_{\text{o pp}}=7.5 \text{ V}$	0.993, 4.57%
3000	$\Delta T_{\text{st}}=200 \text{ ms}$, $\Delta V_{\text{o pp}}=8.75 \text{ V}$	$\Delta T_{\text{st}}=260 \text{ ms}$, $\Delta V_{\text{o pp}}=8.75 \text{ V}$	0.992, 5.00%
2400	$\Delta T_{\text{st}}=200 \text{ ms}$, $\Delta V_{\text{o pp}}=10.0 \text{ V}$	$\Delta T_{\text{st}}=220 \text{ ms}$, $\Delta V_{\text{o pp}}=10.0 \text{ V}$	0.992, 5.02%
2000	$\Delta T_{\text{st}}=200 \text{ ms}$, $\Delta V_{\text{o pp}}=11.0 \text{ V}$	$\Delta T_{\text{st}}=170 \text{ ms}$, $\Delta V_{\text{o pp}}=10.0 \text{ V}$	0.992, 5.10%
1640	$\Delta T_{\text{st}}=200 \text{ ms}$, $\Delta V_{\text{o pp}}=11.5 \text{ V}$	$\Delta T_{\text{st}}=170 \text{ ms}$, $\Delta V_{\text{o pp}}=11.5 \text{ V}$	0.991, 5.45%
1360	$\Delta T_{\text{st}}=180 \text{ ms}$, $\Delta V_{\text{o pp}}=11.87 \text{ V}$	$\Delta T_{\text{st}}=200 \text{ ms}$, $\Delta V_{\text{o pp}}=11.25 \text{ V}$	0.990, 5.88%
940	$\Delta T_{\text{st}}=180 \text{ ms}$, $\Delta V_{\text{o pp}}=15.0 \text{ V}$	$\Delta T_{\text{st}}=180 \text{ ms}$, $\Delta V_{\text{o pp}}=12.5 \text{ V}$	0.991, 5.63%
660	$\Delta T_{\text{st}}=160 \text{ ms}$, $\Delta V_{\text{o pp}}=15.0 \text{ V}$	$\Delta T_{\text{st}}=160 \text{ ms}$, $\Delta V_{\text{o pp}}=15.0 \text{ V}$	0.992, 5.20%
440	$\Delta T_{\text{st}}=160 \text{ ms}$, $\Delta V_{\text{o pp}}=20 \text{ V}$	$\Delta T_{\text{st}}=160 \text{ ms}$, $\Delta V_{\text{o pp}}=17.5 \text{ V}$	0.991, 5.56%

mental measurement is a direct method to observe the behavior of the DCM pre-regulator with the expanded voltage control loop. The measurements have been carried out by means of a real time frequency response analyzer NF FAR5097 and represented with GNU PLOT software. The measured gain of the closed-loop DCM pre-regulator with both the expanded voltage control loop and the standard voltage control loop is shown in Fig. 13. The measurement conditions are that the output power is 100 W and the input voltage is $155 V_{\text{dc}}$. According to the observation from Fig. 13, the gain bandwidth of the DCM pre-regulator is much better with the expanded voltage control loop than with the standard one. Note that the expanded voltage control loop with the notch filter can attenuate the gain at 120 Hz (the second harmonic of the ac mains frequency).

Finally, in order to verify the PFC function of the pre-regulator with the expanded bandwidth voltage control loop, the current harmonic distortions are measured for different output power level, as shown in Fig. 14. The input voltage and the filtered input current at 100 W output power are shown in Fig. 15.

V. CONCLUSION

This paper describes a simple analog circuit implementation to improve the load transient response of power-factor pre-regulator. The analog notch filter is inserted between the output voltage of the pre-regulator and the voltage error amplifier of the pre-regulator control circuitry. This implementation can be applied in existing pre-regulators with minor modification. The notch filter setup in terms of the circuit value is reported. Furthermore a set of measurements on the DCM pre-regulator with different values of the output capacitor using the expanded voltage control loop has been performed. Based on the measurement, the input current harmonic is deteriorated when output capacitor is too small. However, quick response to load disturbances without distorting the input current during steady-state can be achieved. Experimental results show the benefits of this cost-effective solution in improving the load transient response of the pre-regulator.

Fig. 13. Comparison of the gain of the DCM pre-regulator between using the expanded voltage control loop with the notch filter (dash line) and using the standard voltage control loop. (a) The output capacitor value is $4500 \mu\text{F}$.

Fig. 14. Measured harmonic current level of the DCM pre-regulator with the expanded bandwidth voltage control loop with the notch filter. The output capacitor value is $4500 \mu\text{F}$.

Fig. 15. Measured waveforms of the input voltage (upper trace) and the filtered input current (lower trace) at 100 W output power of the DCM pre-regulator with the expanded voltage control loop. The output capacitor value is $4500 \mu\text{F}$.

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