Zero-Order Switching Networks and Their Applications to Power Factor Correction in Switching Converters

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***Abstract*— This paper addresses the requirements of networks containing linear inductors, capacitors and ideal switches for synthesis of zero-order input impedance. Sufficient conditions for achieving zero-order input impedance are stated in terms of the network topology and the switching sequence. Such networks have direct practical relevance to power factor correction (PFC). Based on zero-order switching networks, a comprehensive study is presented for many existing PFC circuits as well as new circuit topologies.**

***Index Terms*— DC/DC converters, graph theory applications, power factor correction, switch mode power supplies.**

I. Introduction

HIGH POWER factor is becoming an increasingly important design criterion for switching power converters in addition to high efficiency. Unity power factor, in the case of a simple one-port network, requires that the phase shift between the voltage and the current be zero, and that the current be free from harmonic distortion. In circuit terms, these requirements call for an input impedance resembling a linear resistor, i.e., a zero-order linear one-port. Although quite a number of switching circuits are already being used in practical power factor correction (PFC), they are scattered in the literature as isolated cases of innovative circuit design [1]–[3]. Moreover, little formal work has been reported on the basic topological requirements of these circuits that can shed light on the creation of new PFC topologies. In this paper we attempt to derive sufficient conditions for which a switching network has a zero-order input impedance. We will also examine some simple zero-order networks that form the basis of a range of PFC circuits being used in practical power supplies. To illustrate the usefulness of the theory, we will derive some "new" possibilities for PFC, by application of duality, which are rarely known to the power electronics engineers.

II. Zero-Order Switching Converter Circuits

Before embarking on a discussion of zero-order networks, the concept of energy storage elements has to be renewed. Specifically, when a capacitor (inductor) forms a loop (cutset) periodically with closed (open) switches, it stores zero energy over one complete switching period. However, within a switching period, it does store energy. Thus, it has no energy storage capability in the low-frequency sense, but remains as a reactive element at switching frequency or higher. As will become apparent, zero-order input impedance is required at low frequencies for PFC. Hence, we may exploit the periodically closed capacitors or opened inductors to create circuits that give zero-order input impedance for low-frequency operations. It should be borne in mind that high-frequency components (near and above switching frequency) are usually removed by filtering, and the main concern is the low-frequency behavior. The essential tool that allows us to focus on the low-frequency behavior is the averaging principle [4], of which we will make free use thoughout the paper.

Switching power converters in general consist of linear inductors, capacitors and ideal switches. The input is typically a voltage source and the output a parallel combination of a capacitor and a load resistor. We now begin with the definitions of topological arrangements that prevent capacitors and inductors from behaving as low-frequency storage elements.

Definition 1: A zero-order switching inductor (L^0) is an inductor which forms a cutset periodically with only open switch(es) and/or current source(s).

Definition 2: A zero-order switching capacitor (C^0) is a capacitor which forms a loop periodically with only closed switch(es) and/or voltage source(s).

Having defined these important elements, we may now formally state our first result concerning the topological requirement of a zero-order network. To avoid confusion, we should stress that a zero-order network does not in general imply a zero-order input impedance, the latter being a subject yet to be examined. (See Section III-C.)

Theorem 1: Suppose all capacitors have finite current and all inductors have finite voltage. A switching converter circuit is zero-order if it is composed of only zero-order switching inductors, zero-order switching capacitors, and switches.

Proof: Since, from the hypothesis, each inductor forms a cutset periodically with open switches and/or current sources, its current is fixed periodically by KCL. Likewise, KVL fixes each capacitor voltage periodically. □

The simplest zero-order switching converter consists of one inductor and two switches. The reason for choosing the inductor (instead of the capacitor) is that the input is a voltage

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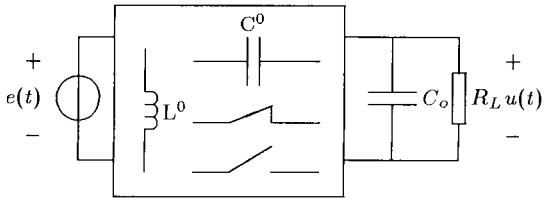


Fig. 1. Zero-order switching converter.

source and the output is a capacitor, both of which can only be switched abruptly onto an inductor (not capacitor). At least two complementary on-off switches are needed because inductor cannot be left open while current is flowing. This leads to three possible topologies which happen to be the well-known buck, buck-boost and boost converters. From Theorem 1, the inductor is required to be an L^0. Hence, there must exist a subinterval in a period for which a cutset is formed exclusively of the inductor and the two open switches. This corresponds to the well-known discontinuous-mode operation.

III. Near Zero-Order Input Impedance and Power Factor Correction

A well established approach to modeling switching converters is via averaging [4], [5]. For example, the input current can be written as the average of the input current observed over one switching period.

$$I_{\text{in}} = \frac{1}{T}\int_0^T i_{\text{in}}(t)\,dt. \tag{1}$$

We are now ready to present the second result concerning the topological requirement of zero-order input impedance.

A. Topological Requirements

Theorem 2: The input impedance of a zero-order switching converter as represented in Fig. 1 is of zero-order if no loop is formed that contains both the input port and the output port for the entire switching period.

Proof: Observe that if there exists no loop containing two branches, b_1 and b_2, of a graph, then the two branches are contained separately in two *disconnected* subgraphs or in two *separable* subgraphs [6]. In particular the current in b_1 and the voltage of b_2 will be independent of each other. Now consider the circuit of Fig. 1. We observe that only the output port voltage involves a storage element. Therefore, the averaged input current in the sense of (1) will not contain a time-derivative term if the hypothesis is true. □

Corollary 1: The buck-boost converter operating in discontinuous mode has a zero-order (i.e., resistive) input impedance. Moreover, both the buck converter and the boost converter operating in discontinuous mode do not have a zero-order impedance.

Proof: By inspection of all three constituent linear networks corresponding to the three switch states of the buck-boost converter, there exists no loop that contains both the input port and the output port (see Fig. 2). Moreover, for the buck and the boost converter, such a loop exists in at least one

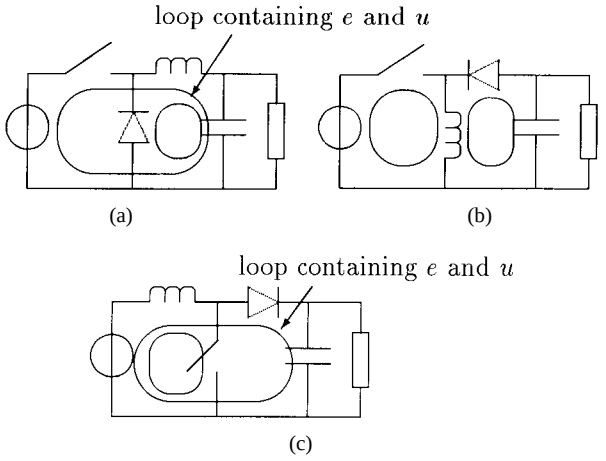


Fig. 2. Corollary 1. (a) Buck converter has a loop that contains input port and output port. (b) Buck-boost converter has no such loops. (c) Boost converter has such a loop.

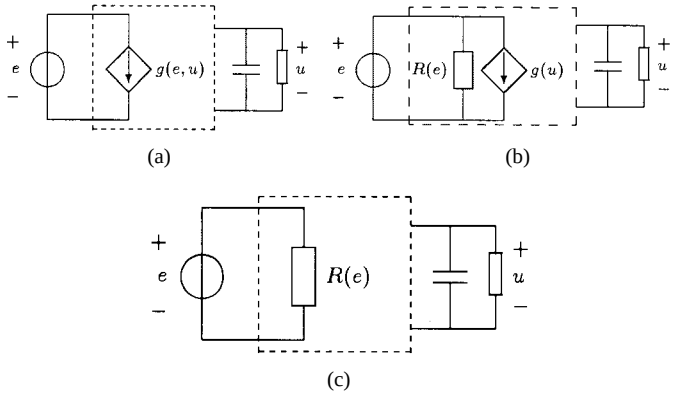


Fig. 3. Averaged models of impedance. (a) General model. (b) Variable separable. (c) zero-order impedance (resistive). Dependence on d and T of all functions omitted for brevity.

subinterval of the switching period. The result follows directly from Theorem 2. □

B Averaged Models for Zero-Order Impedance

Suppose there exists a loop that contains the input port and the output port during a subinterval of the switching period. From basic circuit theory, any voltage or current in a circuit can be written as a function of the input source(s) and the state variable(s). In this case, I_{in} generally depends on both u and e, and if u is a dynamic variable, so is I_{in}. The average model, in general, is a nonlinear controlled current source as shown in Fig. 3(a). If the function $g(\cdot)$ is separable to two terms, each dependent upon one port voltage only, then the model of Fig. 3(b) is valid. Finally, the model reduces to that of Fig. 3(c) for the case where $g(\cdot)$ is independent of u.

For the case of the simple zero-order switching circuits, the input current is given by

$$I_{\text{in}} = \frac{1}{T}\left(\int_0^{dT} i_{\text{in}}(t)\,dt + \int_{dT}^{d'T} i_{\text{in}}(t)\,dt + \int_{d'T}^{T} i_{\text{in}}(t)\,dt\right) \tag{2}$$

where $i_{\text{in}}(t)$ is a function of the input voltage and the output voltage. According to the waveform of the inductor current, we can write down the averaged input current for the three simple converter circuits as

$$\text{Buck converter:} \quad I_{\text{in}} = \frac{d^2T}{2L}(e-u) \tag{3}$$

$$\text{Buck-boost converter:} \quad I_{\text{in}} = \frac{d^2T}{2L}e \tag{4}$$

$$\text{Boost converter:} \quad I_{\text{in}} = \frac{d^2T}{2L}\,\frac{ue}{u-e.} \tag{5}$$

The circuit models for the input impedances are exactly as given in Fig. 3, with (a) corresponding to the boost converter, (b) to the buck converter, and (c) to the buck-boost converter.

C. Application to Power Factor Correction

It should be apparent that any switching converter would have PFC capability if its input impedance is resistive or near resistive. Furthermore, if the input resistance is linear, unity power factor is expected. Thus, from (4), the buck-boost converter operating in discontinuous mode is a perfect choice for PFC if d and T are constant, i.e.,

$$R_{\text{in, buck-boost}} = \frac{2L}{d^2T.} \tag{6}$$

For the buck converter, we can see from (3) that something close to a resistance can indeed be achieved.

$$Z_{\text{in, buck}} = \frac{2L}{d^2T}\left(1+\frac{u}{e}+\frac{u^2}{e^2}+\cdots\right) \tag{7}$$

$$\Rightarrow \quad R_{\text{in, buck}} \approx \frac{2L}{d^2T} \quad \text{if } u \ll e. \tag{8}$$

Likewise, the boost converter can serve as a PFC circuit though not as perfectly as the buck-boost converter. The equivalent resistance can be found as

$$Z_{\text{in, boost}} = \frac{2L}{d^2T}\left(1-\frac{e}{u}\right) \tag{9}$$

$$\Rightarrow \quad R_{\text{on, boost}} \approx \frac{2L}{d^2T} \quad \text{if } u \gg e. \tag{10}$$

Use of the discontinuous-mode boost or buck converter for PFC is expectedly subject to distortion, as can be seen from (7) and (9). (See [2] for a general procedure for deriving the actual power factors and harmonic distortions.) Fortunately, it is possible to compensate for unity power factor in both the buck and the boost converter. Suppose the duty cycle is reserved for some mandatory control function, e.g., voltage regulation in the case of single-stage PFC regulators [1], [2]. Then, the switching frequency becomes the only parameter that may be varied to obtain unity power factor. At this point, a legitimate question arises: Is it possible to derive a frequency control law that can achieve unity power factor? For the simple buck and boost converters, the answer is "yes", since the form of (7) and (9) clearly permits a closed form expression to be written for T in terms of e and u, assuming constant input resistance. Specifically, the control laws required for achieving unity power factor are

$$T = \frac{2L}{d^2R_{\text{in}}}\left(1+\frac{u}{e}+\mathcal{O}\left(\frac{u^2}{e^2}\right)\right) \tag{11}$$

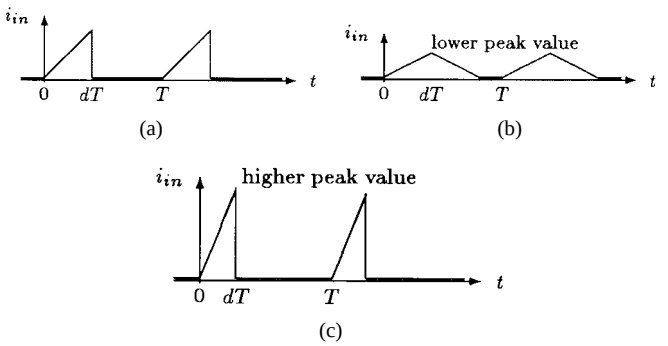


Fig. 4. Input current waveforms comparison. (a) Buck-boost converter. (b) Boost converter (lower peak). (c) Buck converter (higher peak).

for the buck converter, and

$$T = \frac{2L}{d^2R_{\text{in}}}\left(1-\frac{e}{u}\right) \tag{12}$$

for the boost converter, where R_{in} is a constant consistent with the output power. The above idea can be used to improve power factor for discontinuous-mode converters [7].

D. Choice of Topology for Power Factor Correction

Generally speaking, any of the basic converters operating in discontinuous mode can be chosen as a PFC stage, the buck-boost converter being the perfect choice as far as power factor is concerned. However, if we take into account the peak current stress and efficiency, the boost converter is more favorable. First, the lower peak input current, as compared to the buck-boost converter delivering the same amount of power, is easily appreciated by inspecting the typical input current waveforms shown in Fig. 4(a) and (b). Second, the efficiency of the buck-boost converter is usually lower. This is because the input is never coupled directly with the output, and energy is transferred to the load indirectly via circulating loops. Also, as seen from (9), high power factor is possible for the discontinuous-mode boost converter if e/u is small. This means that the switching device must stand a high voltage during its off-state, implying a possible design tradeoff between power factor and voltage stress. As regards the buck converter, high power factor requires small u/e which implies small duty cycle values. The consequence is, however, unfavorably high peak current stress, as illustrated in Fig. 4(c). We may now draw some interim conclusions based on the above discussion:

- The discontinuous-mode buck-boost converter represents a "perfect" PFC stage, but is a less efficient topology.
- The discontinuous-mode boost converter can achieve very high power factor at the expense of high switching device voltage stress. It enjoys low peak current stress.
- The discontinuous-mode buck converter can achieve very high power factor with small duty-cycle values. It suffers high peak current stress.
- The power factor of the discontinuous-mode buck and boost converters can be further improved by application of appropriate frequency control schemes.

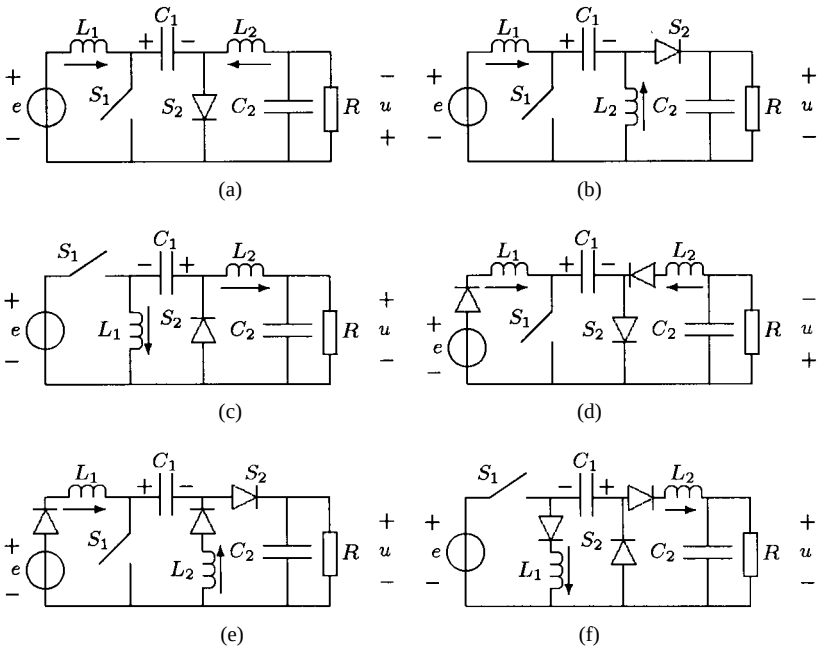


Fig. 5. Higher order converters. (a) Ćuk converter. (b) SEPIC converter. (c) Zeta converter. (d)–(f) Converters with additional diodes to create L^0.

IV. Extension to Higher Order Converters

A. Generalization of Theorem 2

Zero-order switching converters that satisfy the hypothesis of Theorem 2 have a zero-order (resistive) input impedance, and hence are natural unity power factor circuits. Can a higher order switching converter also provide a zero-order input impedance under certain conditions? Intuitively speaking, if the input port "sees" no reactive elements, zero-order input impedance can be maintained. To avoid confusion, we shall refer to an inductor as "reactive inductor" if it is not an L^0, and to a capacitor as "reactive capacitor" if it is not a C^0. Unlike L^0 and C^0 which are not storage elements below switching frequency, "reactive inductors and capacitors" remain as storage elements at all frequencies.

Theorem 3: A general voltage switching converter has a zero-order input impedance if the input port does not form loops with any reactive inductor, reactive capacitor, or the output port.

Proof: The same argument as in the proof of Theorem 2 applies here. The hypothesis implies that the input port branch is, in any subinterval of time, disconnected from all reactive elements. Thus, the input of the converter is resistive. □

The hypothesis of the above theorem essentially means that the input is only allowed to be directly connected to zero-order elements such as L^0 and C^0. The classic example is the buck-boost converter, in which the on-time circulating loop contains the input and an L^0, and the off-time circulating loop contains the L^0 and the reactive output port, the two loops being nonoverlapping in time. In higher order converters, however, the presence of reactive elements play important roles in the energy conversion process. As we shall see later, energy storage capability remains a key property of single-stage PFC regulators. Although one can design to avoid connecting the input with any reactive element by introducing more circulating loops that transfer energy sequentially within a period, the price is poor efficiency. Thus, direct connection between input and reactive elements is often inevitable. The following subsections consider some common examples.

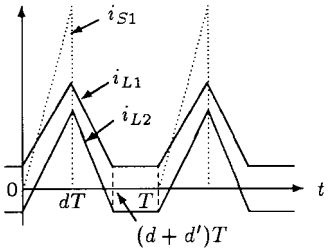
B. The Discontinuous-Mode Ćuk, SEPIC, and Zeta Converters

The Ćuk, SEPIC, and Zeta converters are shown in Fig. 5(a)–(c). Here, unlike in simple converters, the discontinuous-mode operation does not make the inductors behave as L^0. In fact, as shown in Fig. 6(a) the inductor currents do not necessarily touch the zero level although their sum is periodically zero. So, they are still "free to vary" (hence not L^0) although their combined dynamics is reduced to first-order.

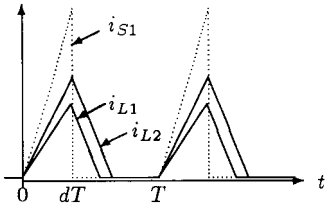
The derivation of the expression for the averaged input current is complicated by the variable diode conduction time. (See [5] for full details.) Moreover, we know that the input impedance is not zero-order because the inductors are not L^0. But high power factor is still possible if the inductor dynamics is negligible.

C. Power Factor Correction by Ćuk, SEPIC, and Zeta Converters

Suppose we can make the inductors, in the Ćuk, SEPIC, and Zeta Converters, behave as L^0. The circuits can then be viewed as some cascade combination of the basic converters in discontinuous mode. This can be accomplished by inserting a diode in series with each inductor, as in Fig. 5(d)–(f). Under such conditions, the inductors are L^0 as illustrated in Fig. 6(b). Clearly, the kind of discontinuous-mode operation differs fundamentally from that described in the previous subsection when series diodes are not present. Note that it is also possible for i_{L_2} to assume continuous-mode operation while keeping



(a)



(b)

Fig. 6. Inductor currents in Ćuk, SEPIC, and Zeta converters operating in discontinuous mode (a) without and (b) with additional diodes in series with inductors.

i_{L_1} discontinuous. We shall deal with this case later in the paper.

We now focus on the Ćuk, SEPIC, and Zeta converters of Fig. 5(d)–(f) operating with both inductors being L^0 [as in Fig. 6(b)]. First, the Ćuk converter's input current is similar to the boost converter's, and can be derived by replacing u with v_{C1} in (5):

$$I_{\text{in,Ćuk}} = \frac{d^2T}{2L_1}\left(\frac{e}{1-\dfrac{e}{v_{C1}}}\right). \tag{13}$$

The input resistance is

$$R_{\text{in,Ćuk}} = \frac{2L_1}{d^2T}\left(1-\frac{e}{v_{C1}}\right) \tag{14}$$

$$\approx \frac{2L_1}{d^2T} \quad \text{if } \left|\frac{e}{v_{C1}}\right| \ll 1. \tag{15}$$

Thus, the Ćuk converter under the specified operating mode can provide PFC if $|e/v_{C1}|$ is small. This again implies a possible tradeoff between voltage stress and power factor.

In a likewise fashion, we can derive, for the SEPIC converter under the specified operating mode, the input current by replacing u with $v_{C1}+u$ in (5), i.e.,

$$I_{\text{in,SEPIC}} = \frac{d^2T}{2L_1}\left(\frac{e}{1-\dfrac{e}{v_{C1}+u}}\right). \tag{16}$$

Hence, we have the input resistance as

$$R_{\text{SEPIC}} = \frac{2L_1}{d^2T}\left(1-\frac{e}{v_{C1}+u}\right) \tag{17}$$

$$\approx \frac{2L_1}{d^2T} \quad \text{if } \left|\frac{e}{v_{C1}+u}\right| \ll 1. \tag{18}$$

Thus, the SEPIC converter can provide PFC if $|e/(v_{C1}+u)|$ is small. Compared to the Ćuk converter, the SEPIC converter seems to suffer less voltage stress since the fact that $u>0$ tends to improve the approximation given in (18).

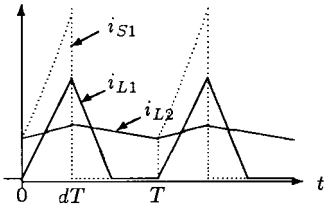


Fig. 7. Current waveforms with L_2 in continuous mode. $i_{\text{in}} = i_{L1}$ for Ćuk and SEPIC. $i_{\text{in}} = i_{S1}$ for Zeta.

For the Zeta converter, the input current when S_1 conducts is the sum of the two inductor currents, and is zero when S_1 is switched off. Thus, the averaged input current, in the specified operating mode, is

$$I_{\text{in,Zeta}} = \frac{d^2T(L_1+L_2)e}{2L_1L_2}\left(1+\frac{L_1}{L_1+L_2}\,\frac{v_{C1}-u}{e}\right). \tag{19}$$

The input resistance is

$$R_{\text{in,Zeta}} = \frac{2L_1L_2}{d^2T(L_1+L_2)}\left[1-\frac{L_1}{L_1+L_2}\,\frac{v_{C1}-u}{e} + \mathcal{O}\left(\left(\frac{L_1}{L_1+L_2}\,\frac{v_{C1}-u}{e}\right)^2\right)\right] \tag{20}$$

$$\approx \frac{2L_1L_2}{d^2T(L_1+L_2)} \quad \text{if } \left|\frac{L_1(v_{C1}-u)}{(L_1+L_2)e}\right| \ll 1. \tag{21}$$

Here, high power factor requires that the magnitude of $L_1(v_{C1}-u)/(L_1+L_2)e$ be small. This remains a fairly weak condition since the factor $L_1/(L_1+L_2)$ further reduces the magnitude of $(v_{C1}-u)/e$.

Remarks: As mentioned before, it is possible that L_2 operates in continuous mode while L_1 in discontinuous mode. This situation may or may not affect the PFC property depending upon the topology. For the Ćuk and SEPIC converters, the input current is actually i_{L1} which is independent of i_{L2}. As long as L_1 remains in discontinuous mode [Fig. 6(b)], the input is still nearly resistive. However, for the Zeta converter, operating L_2 in continuous mode will affect the input current as shown in Fig. 7. Specifically, during the interval when S_1 is on, the input port is connected to L_2 which is not an L^0. Thus, from Theorem 3, the Zeta converter must lose its PFC capability.

V. Switching Regulators with Power Factor Correction

Most commercial applications require the combined use of a PFC circuit and a voltage regulator to provide high input power factor and a fast regulation of output voltage. A straightforward construction involves a simple zero-order switching network followed by a switching regulator. Fig. 8 shows the block diagram of such a circuit.

A. Energy Balance Consideration

In the following analysis we assume that the input voltage is a rectified sinusoid, the power factor is maintained unity, and

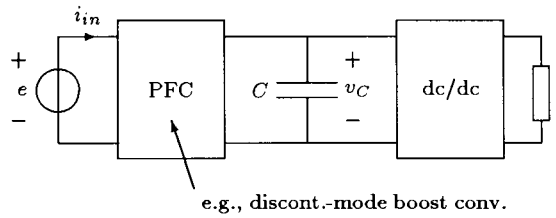


Fig. 8. Block diagram of a two-converter PFC voltage regulator.

the output voltage is constant. The instantaneous input power is $p_{\text{in}}(t) = \hat{e}\hat{i}_{\text{in}} \sin^2 2\pi f_m t$, where f_m is the mains frequency, usually 50 or 60 Hz. Letting P_o be the output power, we have $\hat{e}\hat{i}_{\text{in}} = 2P_o$. The power difference that must be buffered in the circuit is $p_c(t) = \hat{e}\hat{i}_{\text{in}} \sin^2 2\pi f_m t - P_o = -P_o \cos 4\pi f_m t$ which varies at twice the mains frequency. In terms of energy storage, the circuit absorbs energy in a quarter mains cycle and releases the same amount in the next quarter cycle, i.e.,

$$E(t) = -\frac{P_o}{4\pi f_m} \sin 4\pi f_m t + \text{const.} \tag{22}$$

The amplitude (peak-to-peak) of the ac component of the energy stored $|\Delta E_{\text{pp}}|$ is thus given by

$$|\Delta E_{\text{pp}}| = \frac{P_o}{4\pi f_m} \times 2 \tag{23}$$

In the circuit of Fig. 8, the capacitor voltage that interfaces the two stages must fluctuate in order to provide the energy buffering action, i.e., $v_C = V_C + \Delta v_C$ where V_C is a static value and Δv_C varies at $2f_m$. Since the amplitude of energy stored in the capacitor is $\frac{1}{2}C(v_{C,\max}^2 - v_{C,\min}^2)$ or $CV_C|\Delta v_{C_{\text{pp}}}|$, we have, from (23),

$$|\Delta v_{C_{\text{pp}}}| = \frac{P_o}{2\pi f_m C V_C} \tag{24}$$

where $|\Delta v_{C_{\text{pp}}}|$ is the peak-to-peak variation of v_C. We shall examine the merits of different converters in the light of this formula.

B. Effects of Topology Choice on Regulator Design

Small Δv_C implies that a small duty-cycle variation is sufficient for voltage regulation in the dc/dc converter that follows the PFC stage. Small Δv_C is a desirable feature because:

1) Small duty-cycle variation improves the dynamic range and widens the design headroom especially for applications involving a large input voltage range
2) Wide duty-cycle variation can disrupt the PFC property since the equivalent input resistance is a function of d^2T.

From (24), we observe that Δv_C can be made small if V_C is allowed to take a large value. Thus, we can appreciate that the boost (step-up) PFC converter can give small Δv_C and hence facilitate the design of the subsequent voltage regulator, while the buck (step-down) PFC converter is a poor choice since it gives large Δv_C.

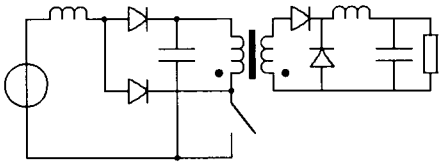


Fig. 9. Cascade of a boost converter and a buck converter to form a single-stage PFC regulator.

TABLE I
SOME KNOWN SINGLE-STAGE PFC REGULATORS

Basic combinations	Operating modes	Circuits
Boost + Buck (Ćuk derived)	DM-CM	BIBRED (ref. [3])
Boost + Buck (Ćuk derived)	DM-DM	SSIPP (ref. [1])
SEPIC derived	DM-CM	BIFRED (ref. [3])
Boost + Flyback	DM-DM	SSIPP (ref. [1])

C. Single-Stage PFC Voltage Regulators

A common practice in the design of PFC voltage regulator is to combine the two converter stages as shown in Fig. 8 to a single stage, especially for low-cost low-power applications. By definition, a single-stage converter employs only one driving signal for turning on and off a switch or a set of switches with a synchronized switching sequence [1]–[3]. An example is shown in Fig. 9 which combines a boost and a buck converter. In theory, provided the front-end converter operates in discontinuous mode, PFC is naturally achieved by virtue of its near zero-order input impedance. Table I summarizes some previously reported configurations.

Our first observation concerns the static value V_C. Two cases can be distinguished: 1) the PFC stage is in discontinuous mode and the subsequent dc/dc converter in continuous mode (DM-CM); 2) both stages are in discontinuous mode (DM-DM).

When operating in DM-DM, the single-stage converter has a fixed static V_C, for a given input voltage function and regulated output voltage, irrespective of the power level or loading condition. We sketch the proof as follows. The input and output currents of any basic discontinuous-mode converter I_{DM} invariably take the following form:

$$I_{\text{DM}} = d^2 T f(v_{\text{in}}, v_{\text{out}}) \tag{25}$$

where v_{in} and v_{out} are the input and output voltages of the converter, and $f(\cdot)$ is usually a bilinear function. Thus, for the circuit of Fig. 8, the current supplied by the PFC stage $I_{o,\text{PFC}}$ and that demanded by the dc/dc converter stage $I_{\text{in,DC/DC}}$ are given by $I_{o,\text{PFC}} = d^2 T f_1(e, v_C)$ and $I_{\text{in,DC/DC}} = d^2 T f_2(v_C, u)$. Also, the averaged current that flows in the storage capacitor over one mains cycle must equal zero, i.e.,

$$\int_0^{1/f_m} d^2 T (f_1(e, v_C) - f_2(v_C, u))\, dt = 0. \tag{26}$$

TABLE II
COMPARISON OF OPERATION MODES IN SINGLE-STAGE PFC REGULATORS

Operation	V_C	Control
DM-DM	Fixed	d control for regulation; f control not feasible for p.f. improvement.
DM-CM	V_C drops as load increases	d control for regulation; f control feasible for p.f. improvement and stress reduction.

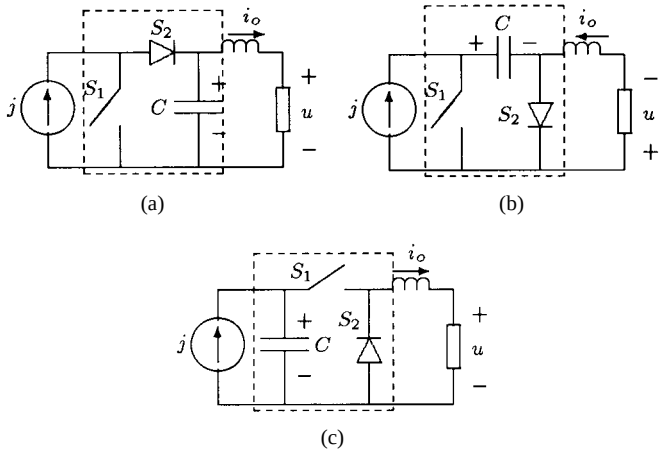


Fig. 10. Zero-order and near zero-order switching converters based on C^0. Direct duals of (a) buck. (b) Buck-boost. (c) Boost converters.

If $\Delta v_C/V_C$ is small and the output is well regulated at U, the duty cycle essentially remains constant. Thus, we may write

$$\int_0^{1/f_m} (f_1(e, V_C) - f_2(V_C, U))\, dt = 0. \tag{27}$$

The above equation clearly suggests that V_C will be invariant under different loading conditions for a given set of e and U.

In contrast, when the single-stage converter operates in DM-CM, the static capacitor voltage V_C varies according to the loading current. We can prove this statement by contradiction. First, we assume that V_C is invariant under two different loading conditions which means that the duty cycle is the same for the two cases since the output remains regulated. From (25), the input current is also invariant under the two loading conditions, which cannot be true. Thus, V_C is expected to take different values for different load currents.

Furthermore, in the case of DM-CM operation, the voltage stress V_C can be controlled by varying the switching frequency since the current charging the storage capacitor $I_{o,\mathrm{PFC}}$ is proportional to d^2T. Thus, increasing the frequency can alleviate the voltage stress on the storage capacitor when the load current becomes small [8].

Our next observation concerns the effects of the choice of operating mode on voltage regulation. With only one switch or one set of switches controlling both PFC and dc/dc stages, the single-stage PFC regulator has the following interesting characteristics. (See Table II.)

1) For DM-DM operation, the use of frequency control for improving power factor can disrupt the voltage regulation because unity power factor is in conflict with the requirement of a constant d^2T for output voltage regulation.
2) Since the continuous-mode converter is not affected by variation of switching frequency, DM-CM operation allows frequency modulation to be used exclusively for improving power factor and duty-cycle modulation for voltage regulation.
3) For DM-CM operation, the switching frequency can be varied according to the loading condition to control the static voltage stress.

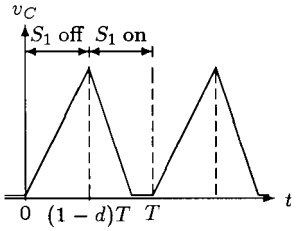


Fig. 11. Capacitor voltage waveform for circuits of Fig. 10.

VI. DERIVATION OF NEW TOPOLOGIES BY THE DUALITY PRINCIPLE

Much has been said about zero-order switching converters which are based on zero-order switching inductors, L^0. Would it be possible to develop new topologies based on zero-order switching capacitors, C^0? This section examines such possibilities.

A. Near Zero-Order Switching Converters Based on Zero-Order Switching Capacitors

A short-cut to the design of C^0-based PFC circuits is via duality transformation. Fig. 10 shows the duals of the basic converter circuits. Note that duality effectively reverses the switch state, i.e., "on" becomes "off", and vice versa. Therefore, if we employ the same definition for duty cycle (percentage of time duration when active switch is on), the discontinuous-mode operation is characterized by zero capacitor voltage during a portion of the on-time as shown in Fig. 11. Since the capacitor C forms a loop periodically with closed switches, it qualifies as a C^0. From Theorem 1, the converters are zero-order switching converters.

Duality allows us to obtain the low-frequency input resistance for the circuits of Fig. 10 by interchanging current and voltage, resistance and conductance, capacitance and inductance, d and $(1-d)$, etc., in previously derived expressions for the buck, buck-boost and boost converters. Specifically, from (7), (6) and (9), the input conductances of the circuits of Fig. 10, in the averaged sense, are given by

$$G_{\mathrm{in,dual\text{-}buck}} = \frac{2C}{(1-d)^2T}\left(1 + \frac{i_o}{j} + \frac{i_o^2}{j^2} + \cdots\right) \tag{28}$$

$$G_{\mathrm{in,dual\text{-}buck\text{-}boost}} = \frac{2C}{(1-d)^2T} \tag{29}$$

$$G_{\mathrm{in,dual\text{-}boost}} = \frac{2C}{(1-d)^2T}\left(1 - \frac{j}{i_o}\right) \tag{30}$$

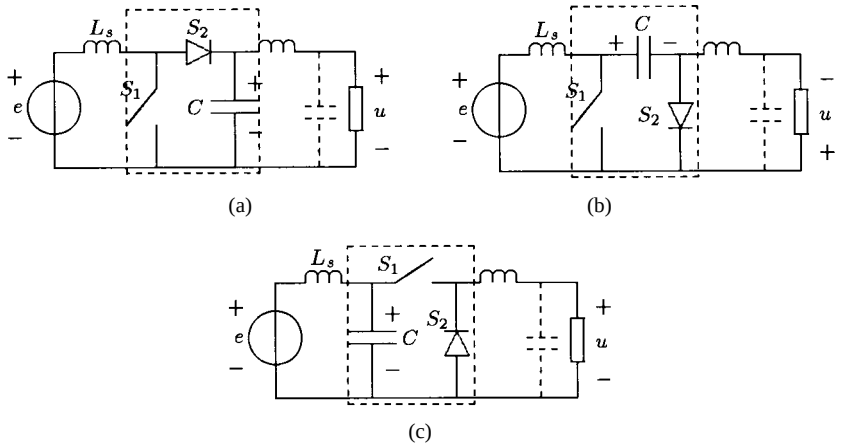


Fig. 12. Modified dual converters for practical source and load. Capacitor C operates in discontinuous mode.

where j and i_o are the input and output currents of the dual converters. Finally, for the sake of conciseness, we state that all conclusions drawn in Section III-D are valid here, provided the appropriate duality translations are made for the involving quantities.

B. Justification of the Current Source Assumption

Although the dual converters (Fig. 10) inherit the PFC property, their suitability for practical applications is questionable because mains inputs are seldom current sources, and regulated voltage is normally required of the output. Thus, the dual circuits necessitate modification in two respects, namely, inserting a "substantial" inductor in the input and plugging a 'small' capacitor on the load as shown in Fig. 12.

From duality, high power factor is maintained only at the input of the dual converter (i.e., dashed box shown in Fig. 12). Thus, the input impedance seen by the voltage source e would have a series inductive component, implying a possible degradation in power factor due to the additional phase shift caused by the inductance. However, if the extent of phase shift is insignificant, these circuits may still be considered.

Since the current source j in the basic dual converters (Fig. 10) is required to remain as a constant current source during a switching period, the rate of change of j should be an order of magnitude lower than the switching frequency. Now observe that $L_s/R_LT = \mathcal{O}(1)$ and $R_{\text{in}}/R_L = \mathcal{O}(1)$, where R_L represents the load resistance. In practice, the mains frequency is several orders of magnitude below the switching frequency, i.e., $\mathcal{O}(f_mT) \ll 1$. Clearly, the phase shift ϕ caused by L_s is given by

$$\tan\,\phi = \frac{2\pi f_m L_s}{R_{\text{in}}} = \frac{2\pi f_m T \dfrac{L_s}{R_L T}}{\dfrac{R_{\text{in}}}{R_L}} = \frac{2\pi \mathcal{O}(f_mT)\mathcal{O}(1)}{\mathcal{O}(1)} = 2\pi\mathcal{O}(f_mT) \ll 1. \quad (31)$$

Thus, we have $\phi \approx \tan\,\phi \ll 1$. In short, due to the wide separation of the mains frequency and the switching frequency, the reactance of L_s can be considered insignificant at the mains frequency, thus justifying the possible use of the dual converters in practical PFC applications.

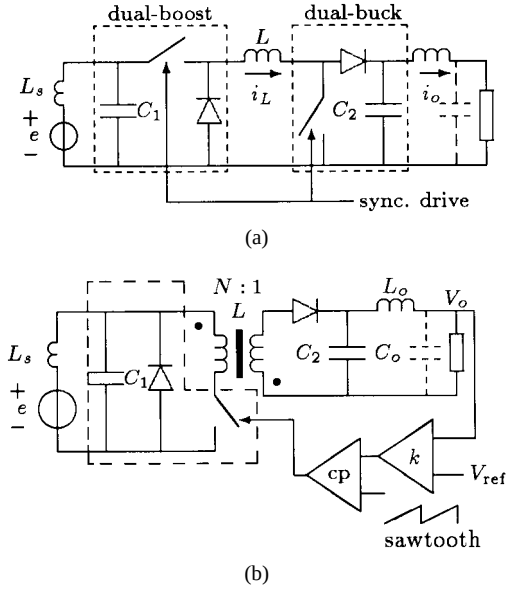


Fig. 13. (a) Dual single-stage PFC regulator with C_1 in discontinuous mode; switches are synchronized for single-stage operation. (b) Isolated version.

C. An Example of Deriving New PFC Voltage Regulator by Duality

In this subsection we illustrate the application of the duality principle to the synthesis of new PFC converters. Specifically, we take the dual of a PFC voltage regulator consisting of a boost and a buck converter. The result is shown in Fig. 13(a). Note that in this dual circuit, the inductor L serves as the low-frequency storage element, whereas the capacitor C_1 is a C^0 providing PFC. Referring to Fig. 13(a), the storage inductor L, in a dual fashion, maintains a continuous current which is larger in magnitude than the input current. The capacitor C_1 operates in discontinuous mode as shown previously in Fig. 11. We refer the readers to Tse-Chow [9] for a detailed analysis of the single-switch isolated version shown in Fig. 13(b).

VII. Conclusion

In this paper we attempt to derive sufficient conditions under which a switching network has a zero-order input impedance. Our discussions have centered around the use of zero-order networks in power factor correction. We should stress that power factor correction may also be achieved by other means since the main theorems presented in this paper provide sufficient conditions only. For example, the boost converter operating in continuous mode contains no L^0 or C^0, and yet can achieve high power factor when a suitable control is applied to shape the input current. Of course, one can logically claim that the inductor somehow must have been prevented from behaving as a reactive element in the low-frequency range [10]. Indeed, such destruction of the low-frequency dynamics remains the necessary condition for achieving power factor correction.

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